9

555 TIMER

9.1 INTRODUCTION

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8-pin circular style, TO-99 can or 8-pin mini DIP or as 14-pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package. A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

The 555 timer can be used with supply voltage in the range of + 5V to + 18V and can drive load upto 200 mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

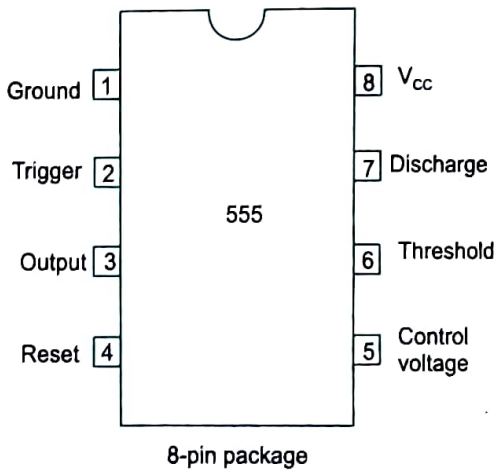

Fig. 9.1 Pin diagram

9.2 DESCRIPTION OF FUNCTIONAL DIAGRAM

Figure 9.1 gives the pin diagram and Fig. 9.2 gives the functional diagram for 555 IC timer. Referring to Fig. 9.2, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) V_{CC} to the upper comparator (UC) and (1/3) V_{CC} to the lower comparator (LC), where V_{CC} is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5). In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

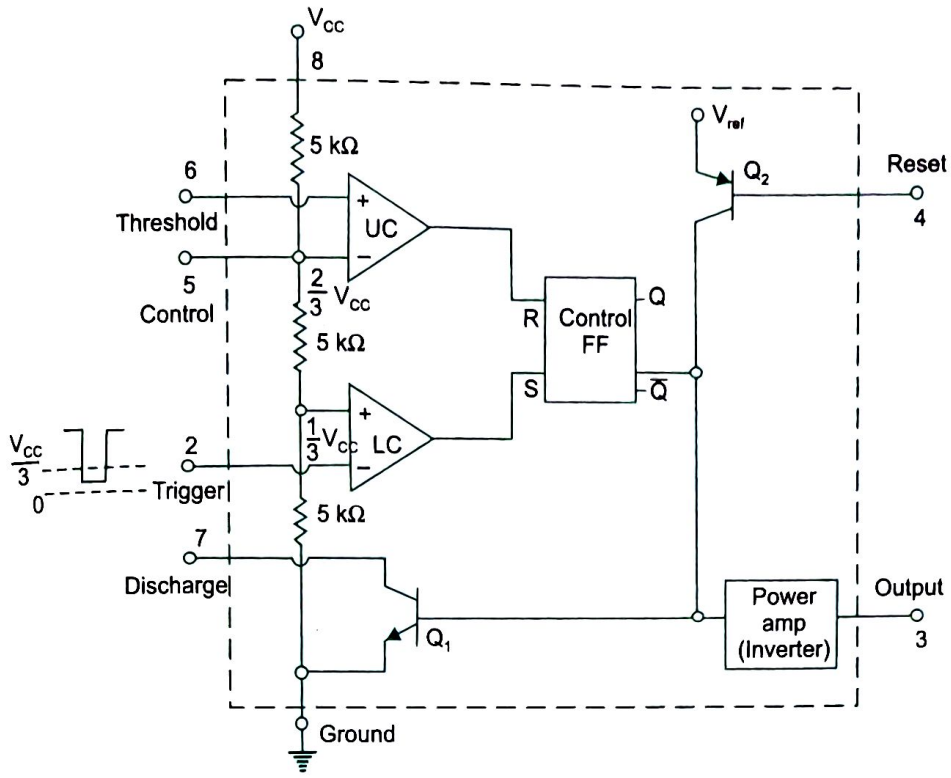

Fig. 9.2 Functional diagram of 555 timer

In the standby (stable) state, the output $\overline{Q}$ of the control flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e. $V_{CC}/3$). At the negative going edge of the trigger, as the trigger passes through ($V_{CC}/3$), the output of the lower comparator goes HIGH and sets the FF ($Q = 1, \overline{Q} = 0$). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3) V_{CC}, the output of the upper comparator goes HIGH and resets the FF ($Q = 0, \overline{Q} = 1$).

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to V_{CC}. The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{CC}.

9.3 MONOSTABLE OPERATION

Figure 9.3 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig. 9.4. In the standby state, FF holds transistor Q_1 ***on***, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e. LOW. As the trigger passes through $V_{CC}/3$, the FF is set, i.e. $\overline{Q} = 0$. This makes the transistor Q_1 ***off*** and the short circuit across the timing capacitor C is released. As $\overline{Q}$ is LOW, output goes HIGH (= V_{CC}). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards V_{CC} with a time constant RC as in Fig. 9.5 (b). After

a time period T (calculated later), the capacitor voltage is just greater than (2/3) V_{CC} and the upper comparator resets the FF, that is, $R = 1$, $S = 0$ (assuming very small trigger pulse width). This makes $\bar{Q} = 1$, transistor Q_1 goes ***on*** (i.e. saturates), thereby discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential as shown in Fig. 9.5 (c).

The voltage across the capacitor as in Fig. 9.5 (b) is given by

$$v_c = V_{CC}\,(1 - e^{-t/RC}) \qquad (9.1)$$

At $t = T$, $\quad v_c = (2/3)\,V_{CC}$

Therefore, $\dfrac{2}{3}V_{CC} = V_{CC}\,(1 - e^{-T/RC})$

or, $\quad T = RC \ln (1/3)$

or, $\quad T = 1.1\,RC$ (seconds) $\qquad (9.2)$

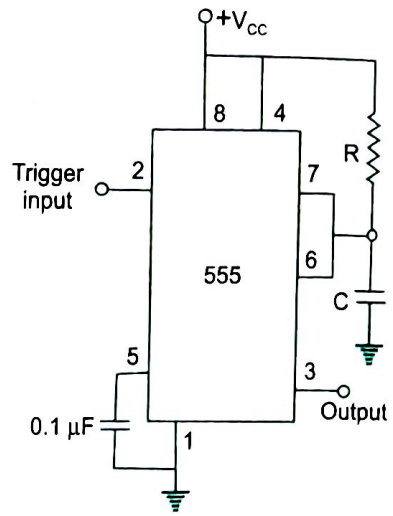

Fig. 9.3 Monostable multivibrator

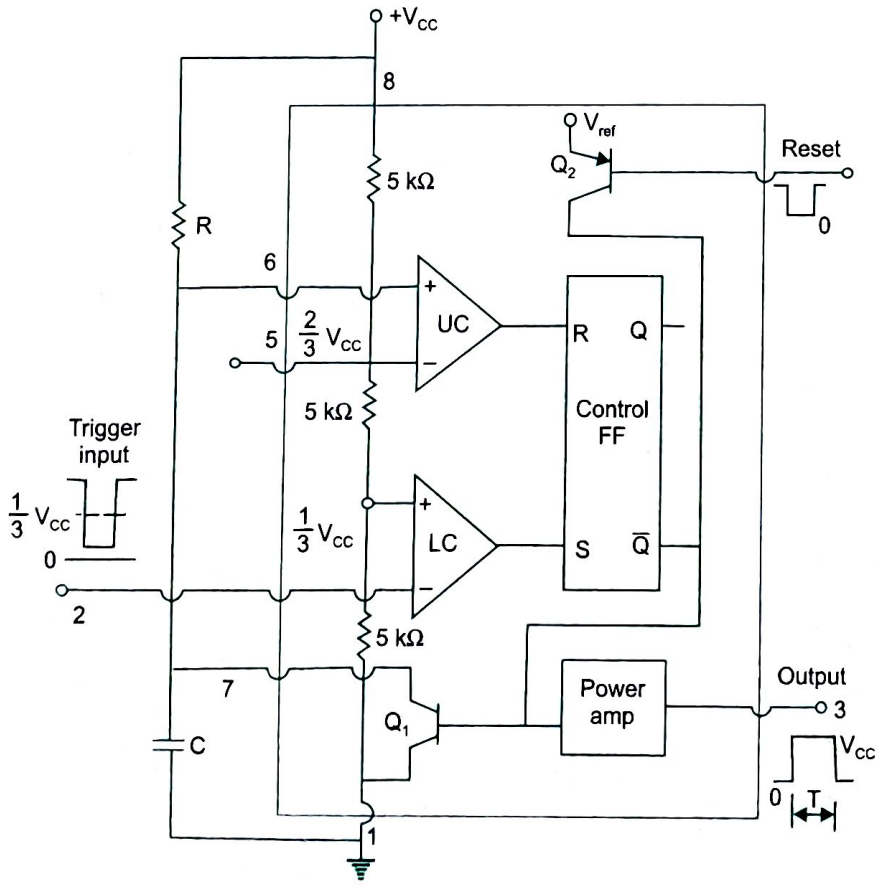

Fig. 9.4 Timer in monostable operation with functional diagram

It is evident from Eq. (9.2) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse as in Fig. 9.5(d) is applied to the reset terminal (pin-4) during the timing cycle, transistor Q_2 goes ***off***, Q_1 becomes ***on*** and the external timing capacitor C is immediately discharged. The output now will be as in Fig. 9.5 (e). It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn ***on*** Q_1 immediately and thereby avoid the propagation delay through the FF. Now, even if the reset is released, the output will still remain LOW until

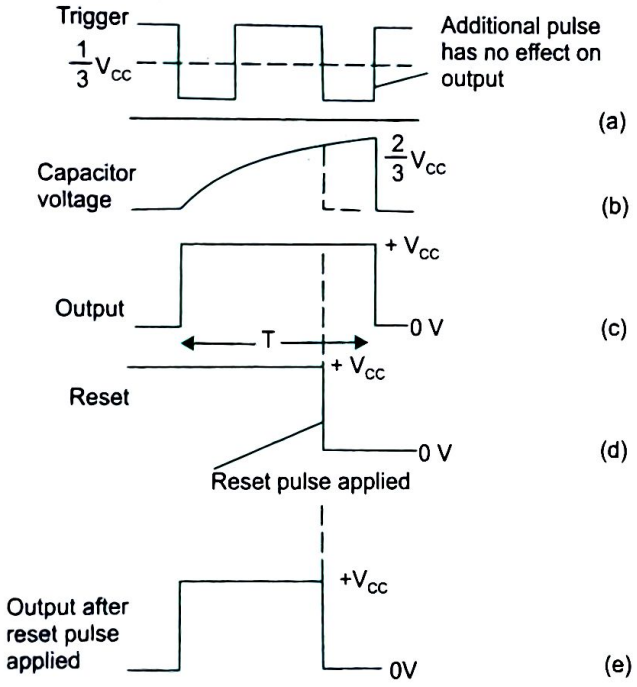

Fig. 9.5 Timing pulses

a negative going trigger pulse is again applied at pin 2. Figure 9.6 shows a graph of the various combinations of R and C necessary to produce a given time delay.

Sometimes the monostable circuit of Fig. 9.3 mistriggers on positive pulse edges, even with the control pin by pass capacitor. To prevent this, a modified circuit as shown in Fig. 9.7 is used. Here the resistor and capacitor combination of 10 kΩ and 0.001 μF at the input forms a differentiator. During the positive going edge of the trigger, diode D becomes forward biased, thereby limiting the amplitude of the positive spike to 0.7 V.

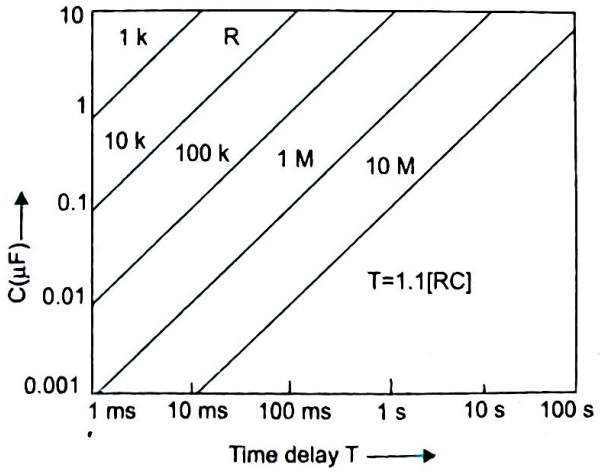

Fig. 9.6 Graph of *RC* combinations for different time delays

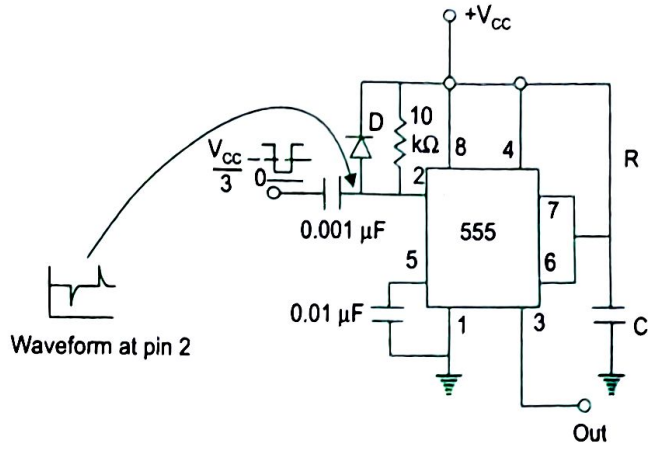

Fig. 9.7 Modified monostable circuit

Example 9.1

In the monostable multivibrator of Fig. 9.3, R = 100 kΩ and the time delay T = 100 mS. Calculate the value of C. Verify the value of C obtained from the graphs of Fig. 9.6.

Solution

From Eq. (9.2), we get

$$C = T/1.1\ R = 100 \times 10^{-3}/1.1 \times 100 \times 10^{3} = 0.9\ \mu F$$

From the graph of Fig. 9.6, the value of C is found to be 0.9 μF also.

9.3.1 Applications in Monostable Mode

Missing Pulse Detector

Missing pulse detector circuit using 555 timer is shown in Fig. 9.8. Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~ 0.7 V). The output of the timer goes HIGH. The circuit is designed so that the time period of the monostable circuit is slightly greater (1/3 longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains HIGH. However, if a pulse misses, the trigger input is high and transistor Q is cut

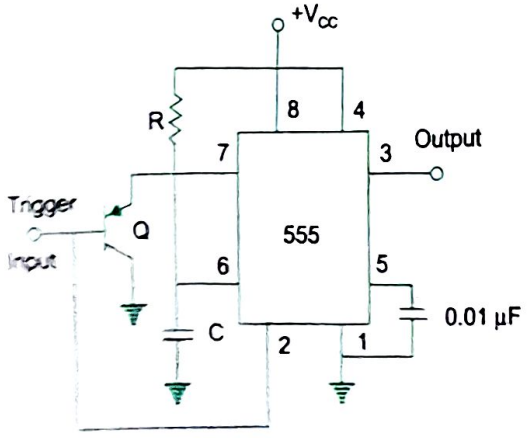

Fig. 9.8 A missing pulse detector monostable circuit

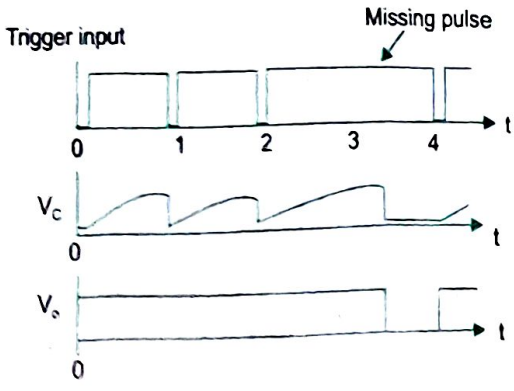

Fig. 9.9 Output of missing pulse detector

off. The 555 timer enters into normal state of monostable operation. The output goes LOW after time T of the mono-shot. Thus this type of circuit can be used to detect missing heartbeat. It can also be used for speed control and measurement. If input trigger pulses are generated from a rotating wheel, the circuit tells when the wheel speed drops below a predetermined value.

Linear Ramp Generator

Linear ramp can be generated by the circuit shown in Fig. 9.10. The resistor R of the monostable circuit is replaced by a constant current source. The capacitor is charged linearly by the constant current source formed by the transistor Q_3. The capacitor voltage v_c can be written as

$$v_c = \frac{1}{C}\int_0^t i\,dt \tag{9.3}$$

where i is the current supplied by the constant current source. Further, the KVL equation can be written as

$$\frac{R_1}{R_1 + R_2} V_{CC} - V_{BE} = (\beta + 1) I_B R_E \approx \beta I_B R_E = I_C R_E = i R_E \tag{9.4}$$

where I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high. Therefore,

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2)} \tag{9.5}$$

Now putting the value of the current i in Eq. 9.3, we get

$$v_c = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{C R_E (R_1 + R_2)} \times t \tag{9.6}$$

At time $t = T$, the capacitor voltage v_c becomes (2/3) V_{CC}. Then we get

$$\frac{2}{3} V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2) C} \times T \tag{9.7}$$

which gives the time period of the linear ramp generator as

$$T = \frac{(2/3) V_{CC} R_E (R_1 + R_2) C}{R_1 V_{CC} - V_{BE}(R_1 + R_2)} \tag{9.8}$$

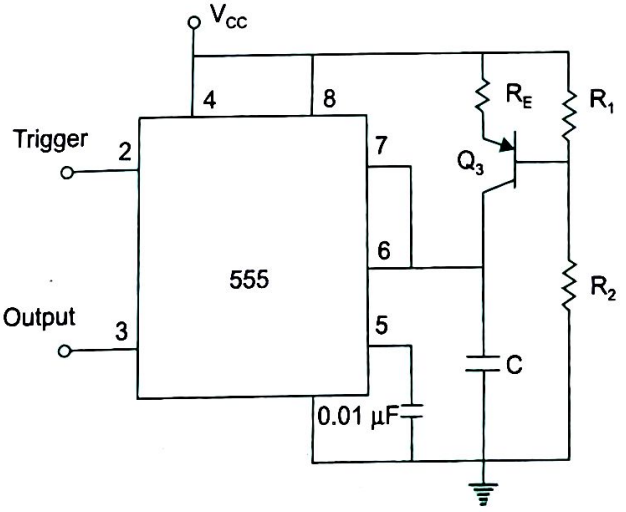

Fig. 9.10 Linear ramp generator

The capacitor discharges as soon as its voltage reaches (2/3) V_{CC} which is the threshold of the upper comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The various waveforms are shown in Fig. 9.11.

The practical values can be noted as

R_1 = 47 kΩ; R_2 = 100 kΩ; R_E = 2.7 kΩ; C = 0.1 μF.
V_{CC} = 5 V (any value between 5 to 18 V can be chosen)

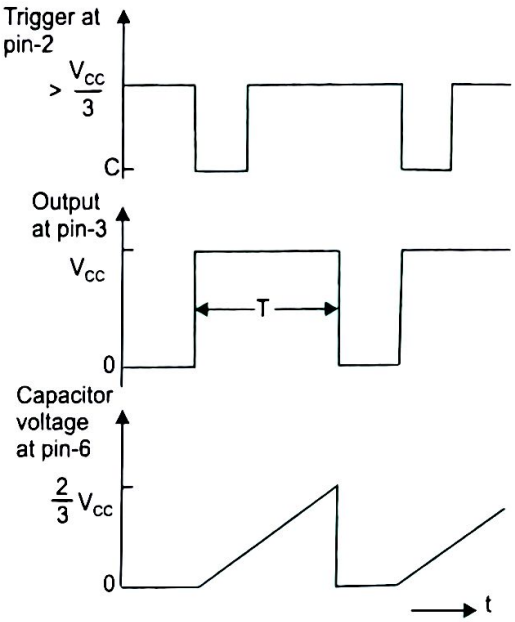

Fig. 9.11 Linear ramp generator output

Frequency Divider

A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal. The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH (because of greater timing interval) for next negative going edge of the input square wave as shown in Fig. 9.12. The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay. In this way, the output can be made integral fractions of the frequency of the input triggering square wave.

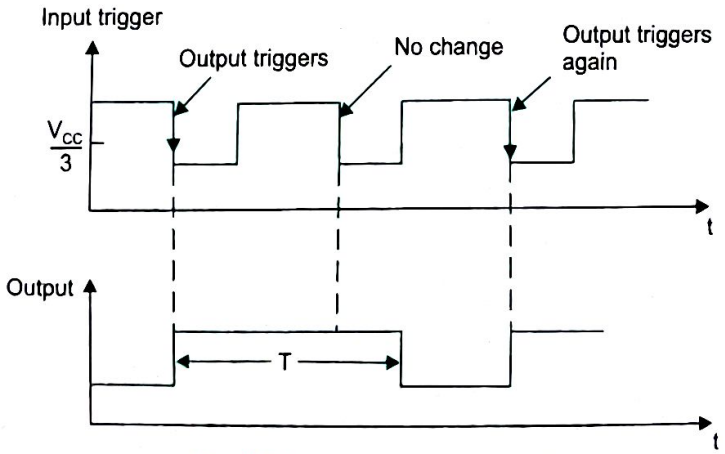

Fig. 9.12 Frequency divider circuit

Pulse Width Modulation

The circuit is shown in Fig. 9.13. This is basically a monostable multivibrator with a modulating input signal applied at pin-5. By the application of continuous trigger at pin-2, a series of output pulses are obtained, the duration of which depends on the modulating input at pin-5. The modulating signal applied at pin-5 gets superimposed upon the already existing voltage (2/3) V_{CC} at the inverting input terminal of UC. This in turn changes the threshold level of UC and the output pulse width modulation takes place. The modulating signal and the output waveform are shown in Fig. 9.14. It may be noted from the output waveform that the pulse duration, that is, the duty cycle only varies, keeping the frequency same as that of the continuous input pulse train trigger.

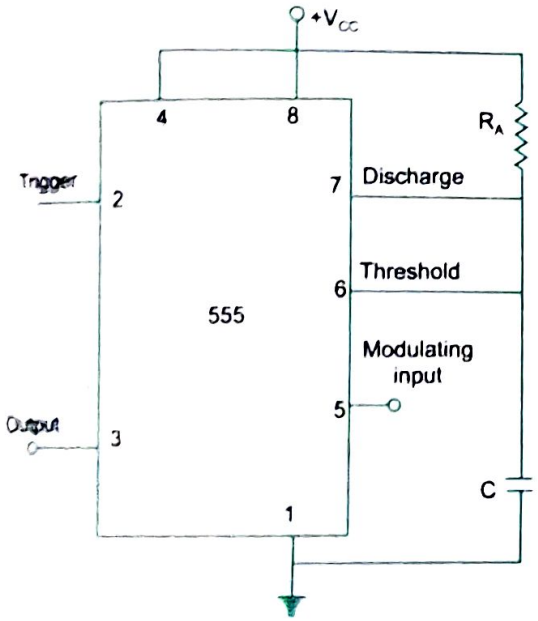

Fig. 9.13 Pulse width modulator

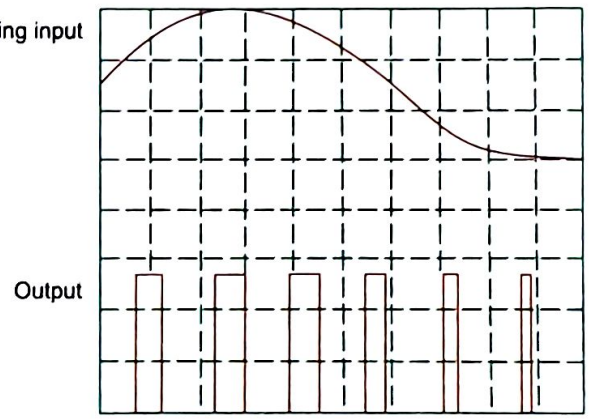

Fig. 9.14 Pulse width modulator waveforms

9.4 ASTABLE OPERATION

The device is connected for astable operation as shown in Fig. 9.15. For better understanding, the complete diagram of astable multivibrator with detailed internal diagram of 555 is shown in Fig. 9.16. Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. When the power supply V_{CC} is connected, the external timing capacitor C charges towards V_{CC} with a time constant $(R_A + R_B)C$. During this time, output (pin 3) is high (equals V_{CC}) as Reset $R = 0$, Set $S = 1$ and this combination makes $\overline{Q} = 0$ which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) V_{CC} the upper comparator triggers the control flip-flop so that $\overline{Q} = 1$. This, in turn, makes transistor Q_1 *on* and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC (neglecting the forward resistance of Q_1). Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1. The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2 A is the maximum current through the *on* transistor Q_1.

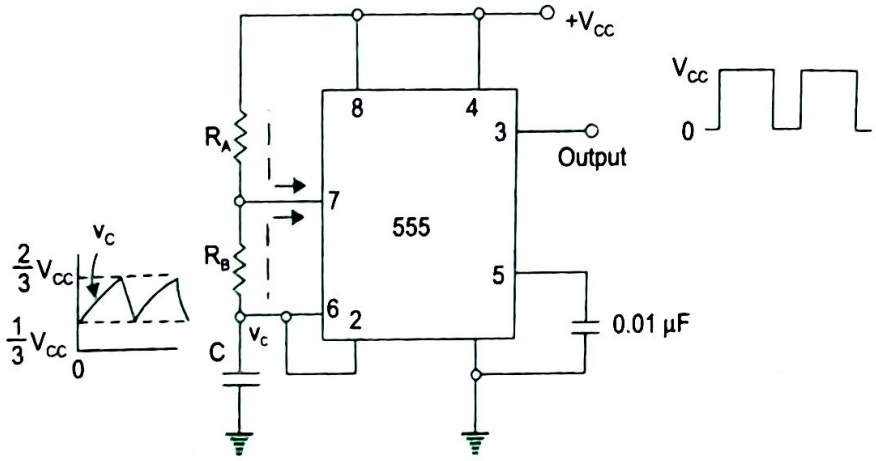

Fig. 9.15 Astable multivibrator using 555 timer

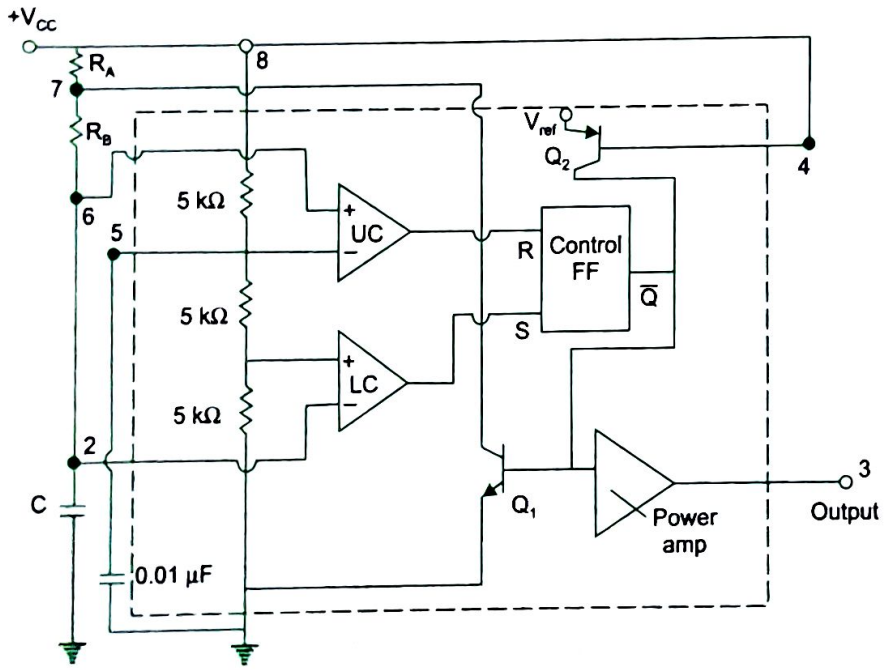

Fig. 9.16 Functional diagram of astable multivibrator using 555 timer

During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) $V_{CC}/3$, the lower comparator is triggered and at this stage $S = 1$, $R = 0$, which turns $\overline{Q} = 0$. Now $\overline{Q} = 0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) V_{CC} and (1/3) V_{CC} respectively. Figure 9.17 shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) V_{CC} to (2/3) V_{CC}. It may be calculated as follows:

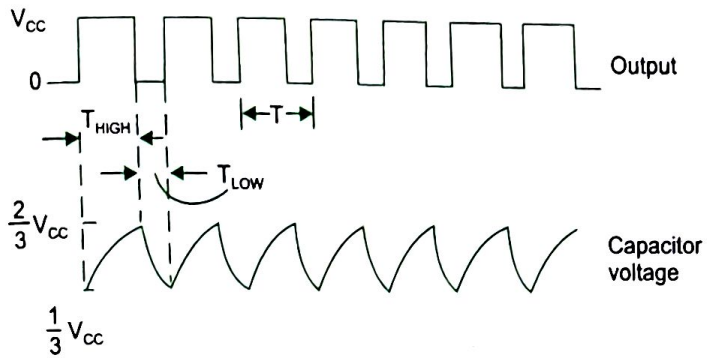

Fig. 9.17 Timing sequence of astable multivibrator

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by

$$v_c = V_{CC}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{CC} is,

$$(2/3)\, V_{CC} = V_{CC}(1 - e^{-t_1/RC}) \tag{9.9}$$

or, $$t_1 = 1.09\, RC$$

and the time t_2 to charge from 0 to (1/3) V_{CC} is,

$$(1/3)\, V_{CC} = V_{CC}(1 - e^{-t_2/RC}) \tag{9.10}$$

or, $$t_2 = 0.405\, RC$$

So the time to charge from (1/3) V_{CC} to (2/3) V_{CC} is

$$t_{HIGH} = t_1 - t_2$$

$$t_{HIGH} = 1.09\, RC - 0.405\, RC = 0.69\, RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\,(R_A + R_B)C \tag{9.11}$$

The output is low while the capacitor discharges from (2/3) V_{CC} to (1/3) V_{CC} and the voltage across the capacitor is given by

$$(1/3)\, V_{CC} = (2/3) V_{CC}\, e^{-t/RC}$$

Solving, we get $t = 0.69\, RC$

So, for the given circuit, $t_{LOW} = 0.69\, R_B C$ (9.12)

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or, $$T = 0.69\,(R_A + 2R_B)\, C$$

So, $$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \tag{9.13}$$

Figure 9.18 shows a graph of the various combinations of $(R_A + 2R_B)$ and C necessary to produce a given stable output frequency. The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$. In this circuit, when the transistor Q_1 is ***on***, the output goes low. Hence,

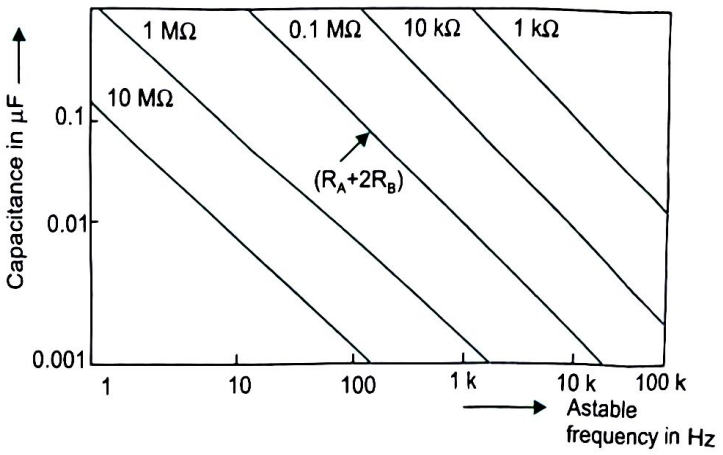

Fig. 9.18 Frequency dependence of R_A, R_B and C

$$D\% = \frac{t_{LOW}}{T} \times 100$$

$$= \frac{R_B}{R_A + 2R_B} \times 100 \qquad (9.14)$$

With the circuit configuration of Fig. 9.15 it is not possible to have a duty cycle more than 50% since $t_{HIGH} = 0.69\ (R_A + R_B)\ C$ will always be greater than $t_{LOW} = 0.69\ R_B\ C$. In order to obtain a symmetrical square wave i.e. $D = 50\%$, the resistance R_A must be reduced to zero. However, now pin 7 is connected directly to V_{CC} and extra current will flow through Q_1 when it is ***on***. This may damage Q_1 and hence the timer.

An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 9.19. During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that

$$t_{HIGH} = 0.69\ R_A C$$

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So $t_{LOW} = 0.69\ R_B\ C$ (9.15)

$$T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + R_B)\ C \qquad (9.16)$$

or, $$f = \frac{1.45}{(R_A + R_B)C} \qquad (9.17)$$

and duty cycle $D = \dfrac{R_B}{R_A + R_B}$

Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width. However, a series resistor of atleast 100 Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value. And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the nonsymmetrical square wave generator is

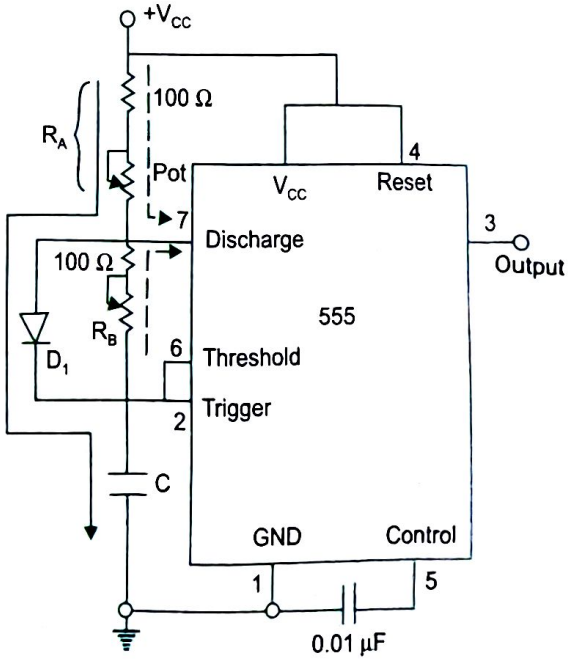

Fig. 9.19 Adjustable duty cycle rectangular wave generator

shown in Fig. 9.20. The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer. The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

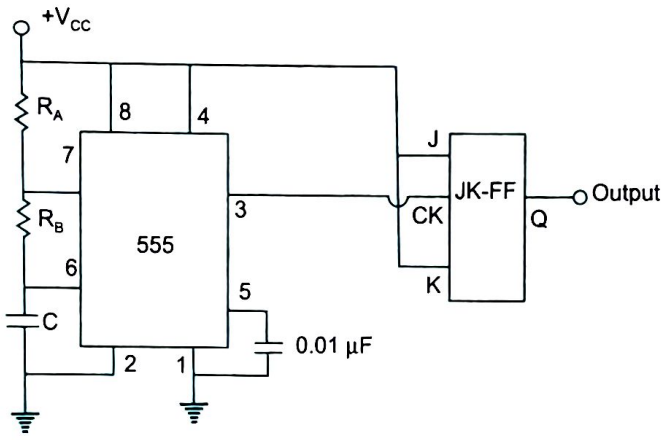

Fig. 9.20 Symmetrical waveform generator

Example 9.2

Refer Fig. 9.15. For $R_A = 6.8\ k\Omega$, $R_B = 3.3\ k\Omega$ and $C = 0.1\ \mu F$, calculate (a) t_{HIGH} (b) t_{LOW} (c) free running frequency (d) duty cycle, D.

Solution

(a) By Eq. (9.11)

$$t_{HIGH} = 0.69\,(6.8\ k\Omega + 3.3\ k\Omega)\,(0.1\ \mu F) = 0.7\ ms$$

(b) By Eq. (9.12)

$$t_{LOW} = 0.69\,(3.3\ k\Omega)\,(0.1\ \mu F) = 0.23\ ms$$

(c) $$f = \frac{1.45}{[(6.8\ k\Omega) + (2)(3.3\ k\Omega)](0.1\ \mu F)} = 1.07\ kHz$$

(d) $$D = \frac{t_{LOW}}{T} = \frac{R_B}{R_A + 2R_B}$$

$$= \frac{3.3\ k\Omega}{6.8\ k\Omega + 2(3.3\ k\Omega)} = 0.25\ or, 25\%$$

9.4.1 Applications in Astable Mode

FSK Generator

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique. A 555 timer in astable mode can be used to generate FSK signal. The circuit is as shown in Fig. 9.21. The standard digital data input frequency is 150 Hz. When input is HIGH, transistor Q is ***off*** and 555 timer works in the normal astable mode of operation. The frequency of the output waveform given by Eq. (9.1) can be rewritten as

$$f_o = \frac{1.45}{(R_A + 2R_B)C} \tag{9.18}$$

In a tele-typewriter using a modulator-demodulator (MODEM), a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals. The components R_A and R_B and the capacitor C can be selected so that f_o is 1070 Hz.

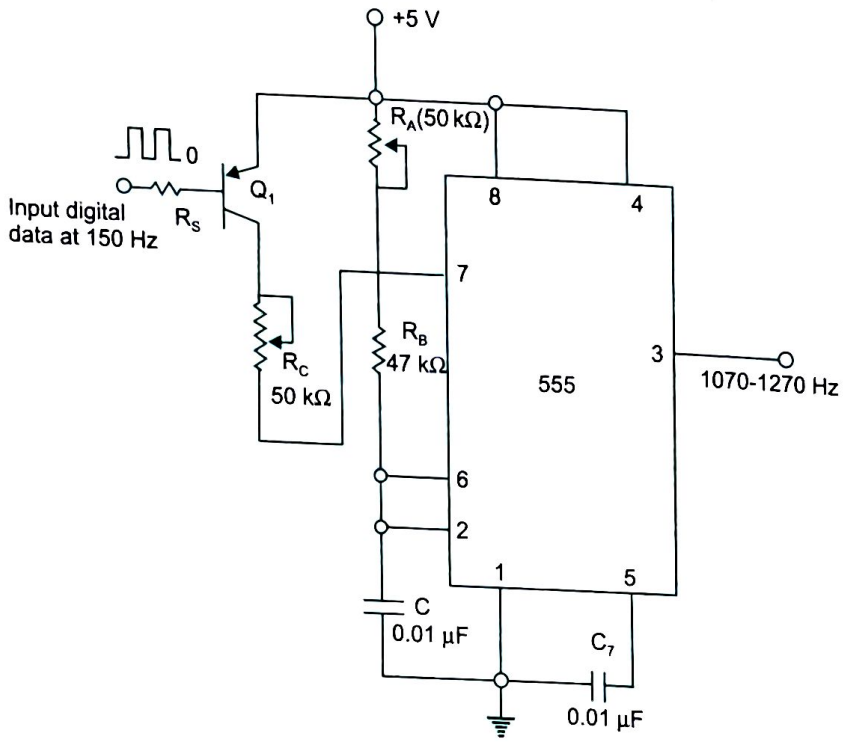

Fig. 9.21 FSK generator

When the input is LOW, Q goes ***on*** and connects the resistance R_C across R_A. The output frequency is now given by

$$\frac{1.45}{(R_A \| R_C) + 2R_B} \tag{9.19}$$

The resistance R_C can be adjusted to get an output frequency 1270 Hz.

Pulse-Position Modulator

The pulse-position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation as shown in Fig. 9.22. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.

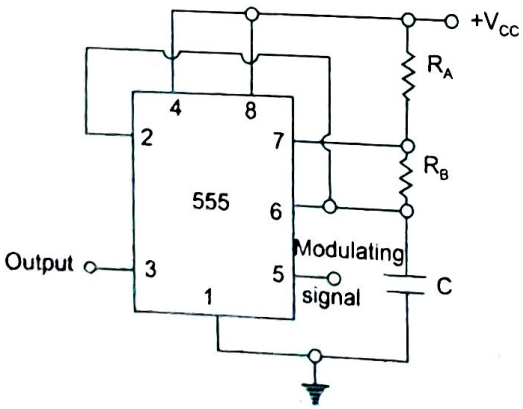

Fig. 9.22 Pulse position modulator

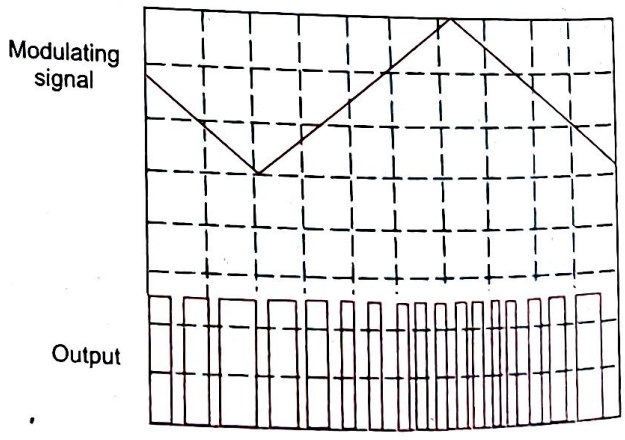

Fig. 9.23 Pulse position modulator output

Figure 9.23 shows the output waveform generated for a triangle wave modulation signal. It may be noted from the output waveform that the frequency is varying leading to pulse position modulation. The typical practical component values may be noted as

R_A = 3.9 kΩ, R_B = 3 kΩ, C = 0.01 μF

V_{CC} = 5 V (any value between 5 V to 18 V may be chosen)

9.5 SCHMITT TRIGGER

The use of 555 timer as a Schmitt Trigger is shown in Fig. 9.24. Here the two internal comparators are tied together and externally biased at $V_{CC}/2$ through R_1 and R_2. Since the upper comparator will trip at (2/3) V_{CC} and lower comparator at (1/3) V_{CC}, the bias provided by R_1 and R_2 is centered within these two thresholds.

Thus, a sine wave of sufficient amplitude (> $V_{CC}/6 = 2/3\ V_{CC} - V_{CC}/2$) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in Fig. 9.25.

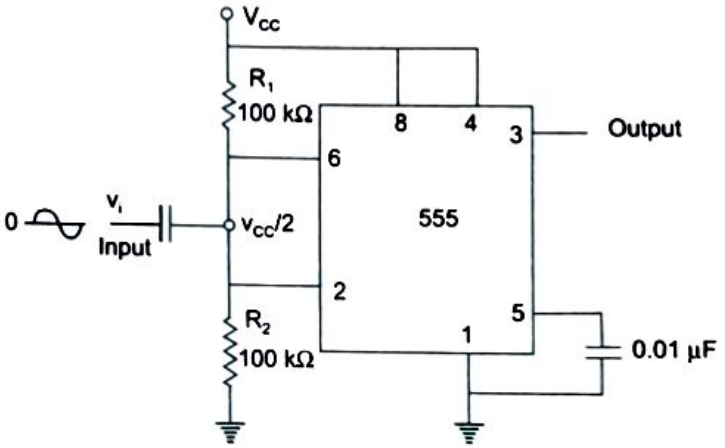

Fig. 9.24 Timer in Schmitt Trigger Operation

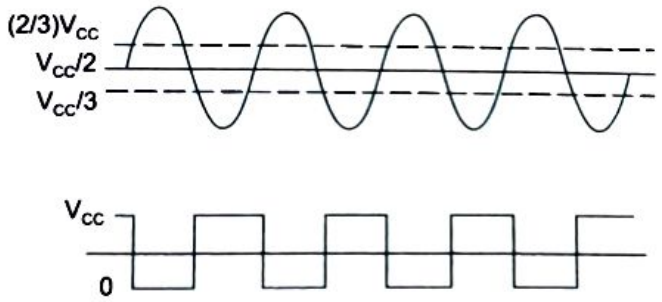

Fig. 9.25 Input output waveforms of Schmitt Trigger

It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square wave remains the same as that of input signal.

SUMMARY

1. 555 IC Timer can produce very accurate and stable time delays, from microseconds to hours.
2. Timer is available in two packages, circular can and DIP.
3. It can be used with supply voltage varying from 5 to 18 V and thus is compatible with TTL and CMOS circuits.
4. Timer can be used in monostable or astable mode of operation. Its various applications include waveform generator, missing pulse detector, frequency divider, pulse width modulator, burglar alarm, FSK generator, ramp generator, pulse position modulator etc.

REVIEW QUESTIONS

9.1. Draw and explain the functional diagram of a 555 Timer.
9.2. Explain the function of reset.
9.3. What are the modes of operation of a timer?
9.4. Derive the expression of time delay of a monostable multivibrator.
9.5. Discuss some applications of timer in monostable mode.
9.6. Define duty cycle D.
9.7. Give methods for obtaining symmetrical square wave.
9.8. Discuss the operation of a FSK generator using 555 timer.
9.9. How is an astable multivibrator connected into a pulse position modulator?
9.10. Draw the circuit of a Schmitt trigger using 555 timer and explain its operation.

PROBLEMS

9.1. Design a monostable multivibrator using 555 timer to produce a pulse width of 100 ms. Verify the values of R and C obtained from the graph of Fig. 9.6.
9.2. The monostable multivibrator of Fig. 9.3 is used as a divide-by-3 network. The frequency of the input trigger is 15 kHz. If the value of C = 0.01 μF, calculate, the value of resistance R.
9.3. In the astable multivibrator of Fig. 9.15, R_A = 2.2 kΩ, R_B = 6.8 kΩ and C = .01 μF. Calculate (i) t_{HIGH} (ii) t_{LOW}, (iii) free running frequency, and (iv) duty cycle D.
9.4. Design a square waveform generator of frequency 100 Hz and duty cycle of 75%.
9.5. Design a symmetrical square waveform generator of 10 kHz.

EXPERIMENT

To construct and observe the waveforms of a 1 kHz square waveform generator using 555 timer for duty cycle, (a) D = 0.25; (b) D = 0.50.

Design Aspects:

(a) Unsymmetrical square waveform generator

$$f = 1 \text{ kHz and } D = 0.25$$

In Fig. 9.15, $$f = \frac{1.45}{(R_A + 2R_B)C}$$

and $$D = \frac{R_B}{R_A + 2R_B}$$

Select $C = 0.1$ μF

Solving for R_A and R_B, we get

$$R_A = 3.6 \text{ kΩ}; \; R_B = 5.5 \text{ kΩ}$$

(b) Symmetrical square waveform generator

$$f = 1 \text{ kHz and } D = 0.50$$

In the circuit of Fig. 9.19

$$f = \frac{1.45}{(R_A + R_B)C}$$

and $$D = \frac{R_B}{R_A + R_B}$$

Select $C = 0.1\ \mu F$

Use a diode 0A79

Solve for R_A and R_B. We get.

$$R_A = R_B = 7.25\ k\Omega$$

PROCEDURE

1. Connect the circuit of Fig. 9.15 using component values as obtained in design part (a).
2. Observe and sketch the capacitor voltage waveform (pin-6) and output waveform (pin-3). Measure the frequency and duty cycle of the output waveform.
3. Next make the circuit of Fig. 9.19 using component values as obtained from design part (b).
4. Repeat step 2.

10

PHASE-LOCKED LOOPS

10.1 INTRODUCTION

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

10.2 BASIC PRINCIPLES

The basic block schematic of the PLL is shown in Fig. 10.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO).

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ components at its output. The high frequency component $(f_s + f_o)$ is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal

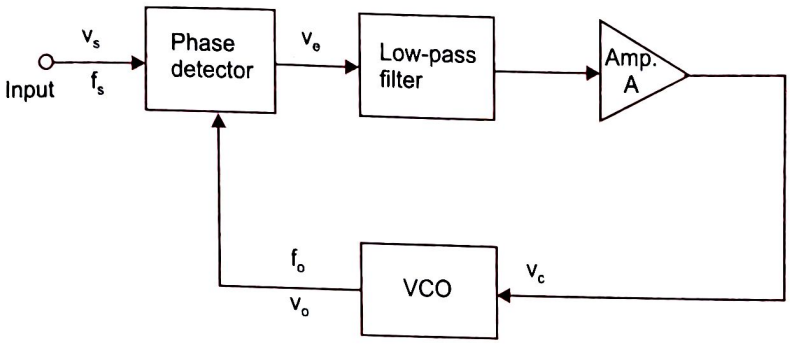

Fig. 10.1 Block schematic of the PLL

frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Figure 10.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o, the VCO frequency.

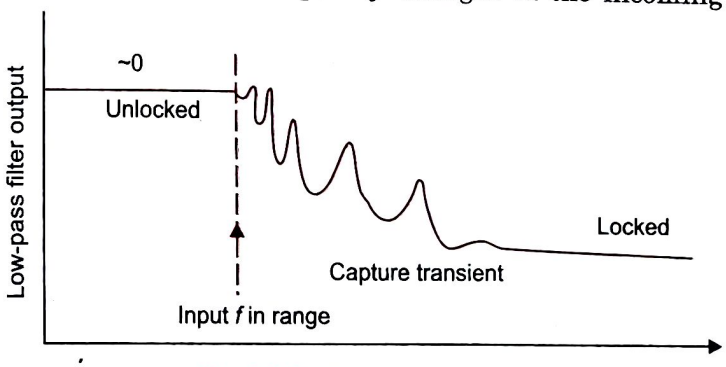

Fig. 10.2 The capture transient

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

10.3 PHASE DETECTOR/COMPARATOR

The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.

10.3.1 Analog Phase Detector

The principle of analog phase detection using switch type phase detector is shown in Fig. 10.3(a). An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) as shown in Fig. 10.3 (b). The input signal is, therefore, chopped at a repetition rate determined by VCO frequency. Figure 10.3 (c) shows the input signal v_s assumed to be in phase ($\phi = 0°$) with

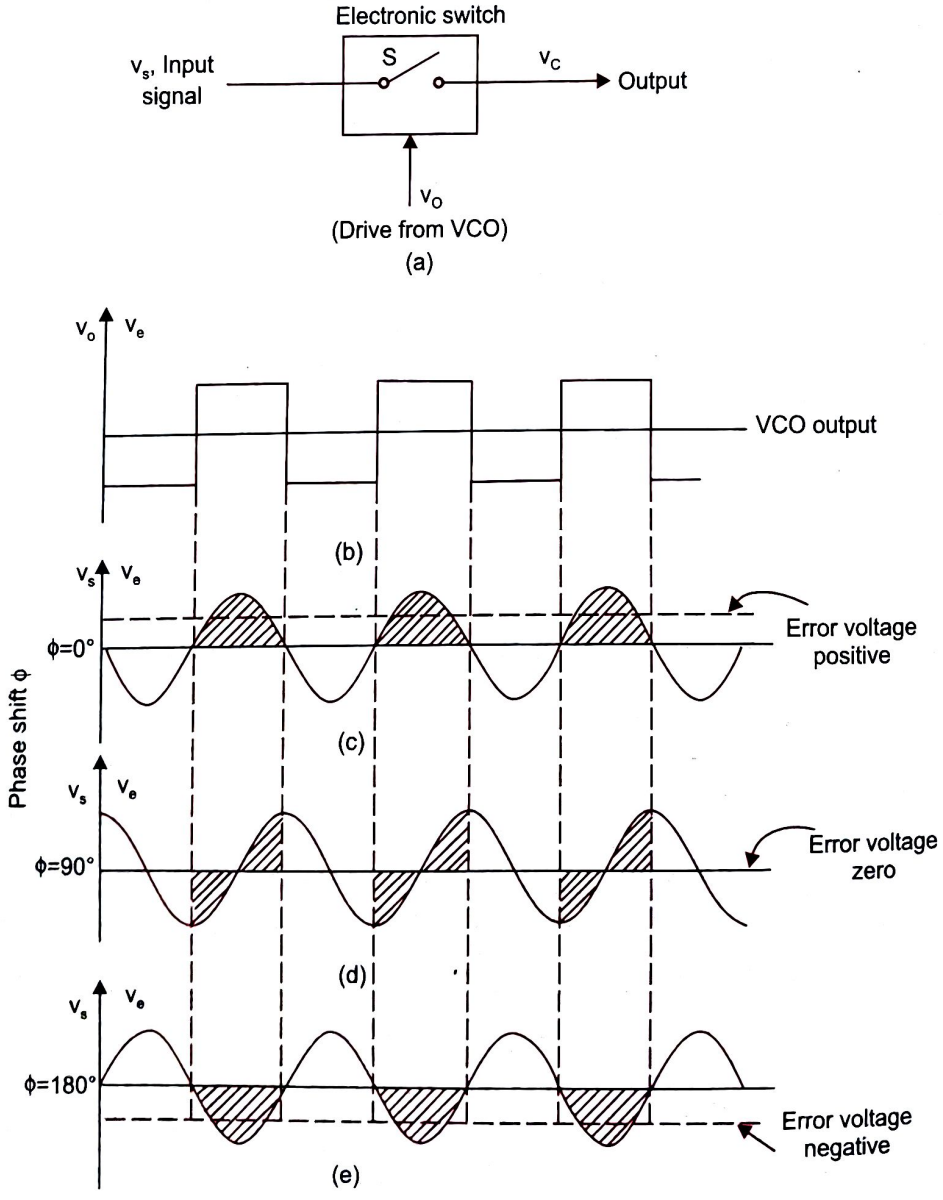

Fig. 10.3 Phase detector for PLL (a) Basic scheme (b) VCO output waveform. Input and output waveform (hatched) of phase detector for (c) $\phi = 0$ (d) $\phi = 90°$ (e) $\phi = 180°$

VCO output v_o. Since the switch S is closed only when VCO output is positive, the output waveform v_e will be half sinusoids (shown hatched). Similarly, the output waveform for $\phi = 90°$ and $\phi = 180°$ is shown in Fig. 10.3 (d, e). This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged. The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in Fig. 10.3 (c, d, e).

It may be seen that the error voltage is zero when the phase shift between the two inputs is 90°. So, for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.

Analysis

A phase comparator is basically a multiplier which multiplies the input signal ($v_s = V_s \sin 2\pi f_s t$) by the VCO signal ($v_o = V_o \sin (2\pi f_o t + \phi)$). Thus the phase comparator output is,

$$v_e = KV_sV_o \sin (2\pi f_s t) \sin (2\pi f_o t + \phi) \tag{10.1}$$

where K is the phase comparator gain (or attenuation constant) and ϕ is the phase shift between the input signal and the VCO output. Equation 10.1 can be simplified as,

$$v_e = \frac{KV_sV_o}{2}\left[\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)\right] \tag{10.2}$$

when at lock, that is, $f_s = f_o$,

$$\text{Then } v_e = \frac{KV_sV_o}{2}\left[\cos(-\phi) - \cos(2\pi \times 2f_o t + \phi)\right] \tag{10.3}$$

This shows that the phase comparator output contains a double frequency term and a dc term $(KV_sV_o/2) \cos \phi$ which varies as a function of phase ϕ, that is, $\cos \phi$ between the two signals. The double frequency term is eliminated by the low pass filter and the dc signal is applied to the modulating input terminal of a VCO. It can be seen that in the perfect locked state ($f_s = f_o$), the phase shift should be 90° ($\cos 90° = 0$), in order to get zero error signal, that is, $v_e = 0$.

There are two problems associated with the switch type phase detector:

1. The output voltage v_e is proportional to the input signal amplitude V_s. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.
2. The output is proportional to $\cos \phi$ and not proportional to ϕ making it non-linear.

Both these problems can be eliminated by limiting the amplitude of the input signal, that is, converting the input to a constant amplitude square wave. A circuit which performs phase comparison with square wave input is shown in Fig. 10.4 (a). This is a balanced modulator used as full-wave switching phase detector. Here the input signal is applied to the differential pair Q_1Q_2. Transistors Q_3–Q_4 and Q_5–Q_6 are two sets of SPDT switches activated by the VCO output. The input signal v_s and the VCO output v_o are assumed to be high enough to switch the transistors in Fig. 10.4 (a) fully ***on*** or ***off***. In Fig. 10.4 (b) when v_s and v_o both are high during the time 0 to $(\pi-\phi)$, transistors Q_1 and Q_3 are driven ***on*** and current I_E flows through Q_1 and Q_3. This gives an output voltage

$$v_e = -I_E R_L \tag{10.4}$$

Next for the period $(\pi - \theta)$ for π, when v_s is high and v_o is low, transistors Q_1 and Q_4 are driven ***on*** resulting in an output voltage

$$v_e = I_E R_L \tag{10.5}$$

In this way, the output voltage waveform v_e in Fig. 10.4 (b) is obtained.

The average value of the phase detector output v_e can be calculated as,

$$(v_e)_{av} = \frac{1}{\pi}[(\text{area } A_1) + (\text{area } A_2)]$$

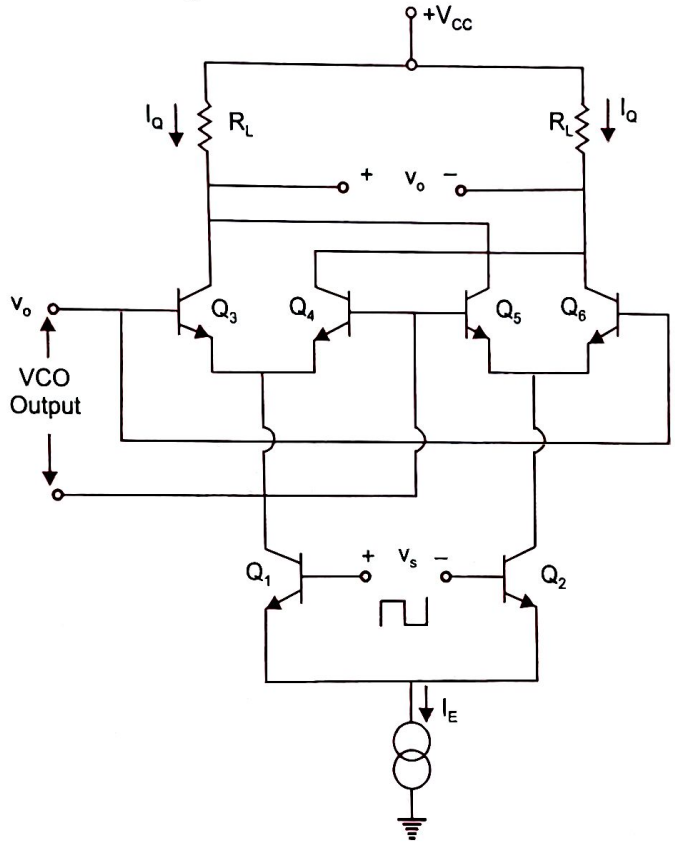

Fig. 10.4 (a) Phase detector for IC PLL

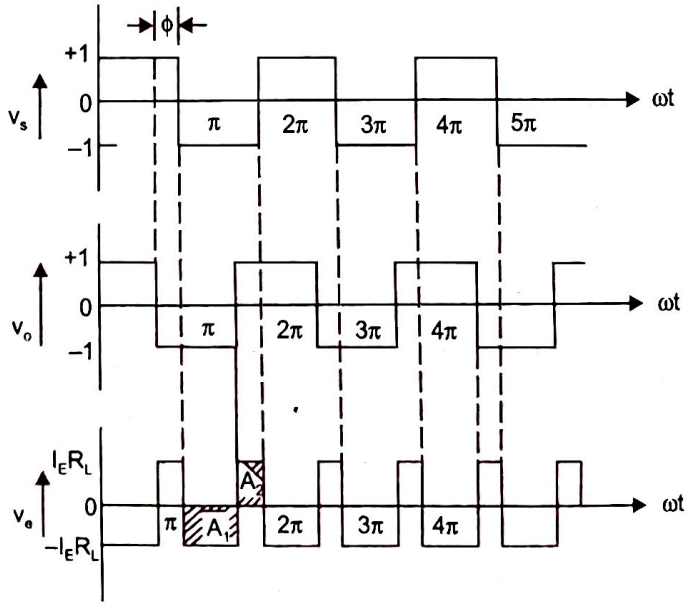

Fig. 10.4 (b) Timing diagram of input and output waveforms for balanced modulator circuit of Fig. 10.4 (a)

$$= \frac{1}{\pi}\left[I_E R_L \phi + (-I_E R_L) \times (\pi - \phi)\right] = I_E R_L \left(\frac{2\phi}{\pi} - 1\right)$$

$$= 4\frac{I_Q R_L}{\pi}\left(\phi - \frac{\pi}{2}\right) \qquad [\text{Since } I_E = 2I_Q]$$

$$= K_\phi(\phi - \pi/2) \tag{10.6}$$

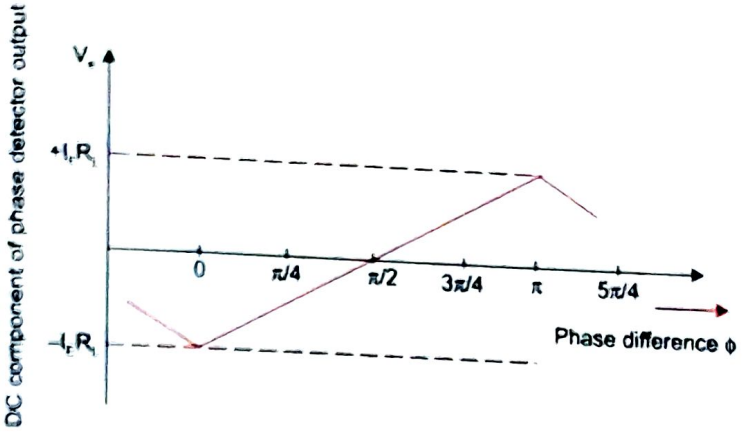

Fig. 10.4 (c) Output dc voltage versus input phase difference of balanced modulator full wave switching phase detector

where K_ϕ is the phase angle-to-voltage transfer coefficient or, the **conversion ratio of the phase detector**. This linear relationship between v_o and ϕ is depicted in Fig. 10.4 (c).

10.3.2 Digital Phase Detector

Figure 10.5 (a) shows the digital type XOR (Exclusive–OR) phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR gate is high when only one of the inputs signals f_s or f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_o$ are shown in Fig. 10.5 (b). In this figure f_s is leading f_o by ϕ degrees. The variation of dc output voltage with phase difference

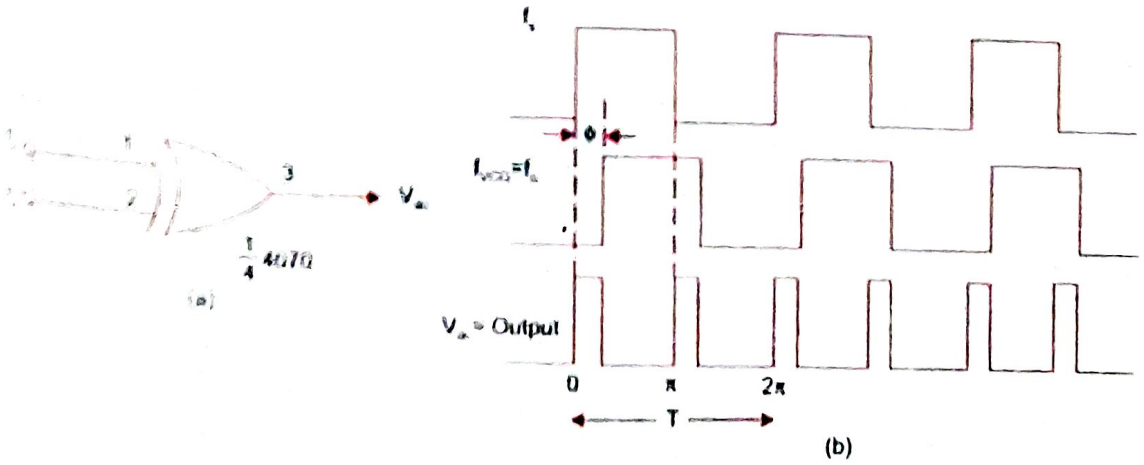

Fig. 10.5 (a) Exclusive-OR phase detector, (b) Input and output waveforms

ϕ is shown in Fig. 10.5 (c). It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout. The slope of the curve gives the conversion ratio k_ϕ of the phase detector. So, the conversion ratio K_ϕ for a supply voltage $V_{CC} = 5$ V is,

$$K_\phi = \frac{5}{\pi} = 1.59 \text{ V/rad} \qquad (10.7)$$

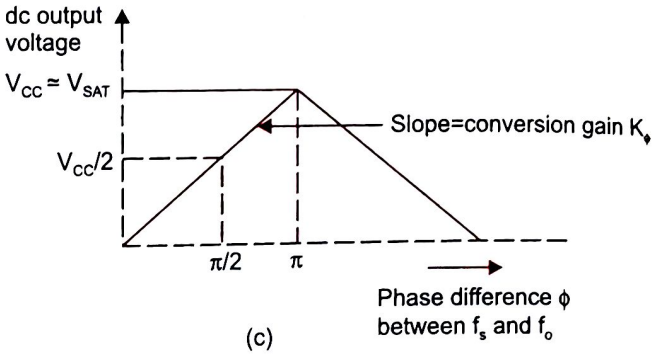

Fig. 10.5 (c) DC output voltage versus phase difference ϕ curve

Another type of digital phase detector is an ***edge-triggered phase detector*** as shown in Fig. 10.6 (a). The circuit is an R-S flip-flop made by NOR gates, such as CD 4001. This circuit is useful when f_s (incoming signal) and f_0 (VCO output) are both pulse waveforms with duty cycle less than 50 per cent. The output of the R-S flip-flop changes its state on the leading edge of f_s and f_0 as shown in Fig. 10.6 (b). The variation of dc output voltage vs phase difference between f_s and f_0 is shown in Fig. 10.6 (c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear upto 360° compared to 180° in the case of Exclusive-OR detector.

Digital phase detector is also available in independent monolithic IC form. A typical example is MC4344/4044. This IC gives input/output transfer characteristics which is linear upto 4π radians or 720°.

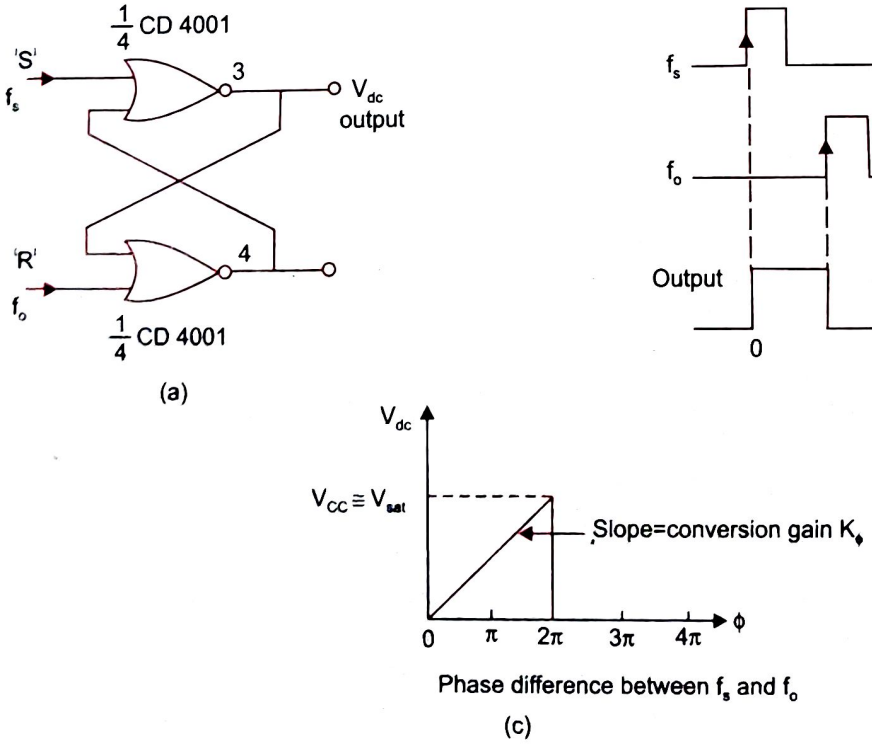

Fig. 10.6 (a) Edge-triggered phase detector using CD4001, Quad 2-input NOR gate, (b) Input and output waveforms, (c) dc output voltage vs phase difference ϕ

10.4 VOLTAGE CONTROLLED OSCILLATOR (VCO)

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 10.7 (a, b). Referring to Fig. 10.7 (b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

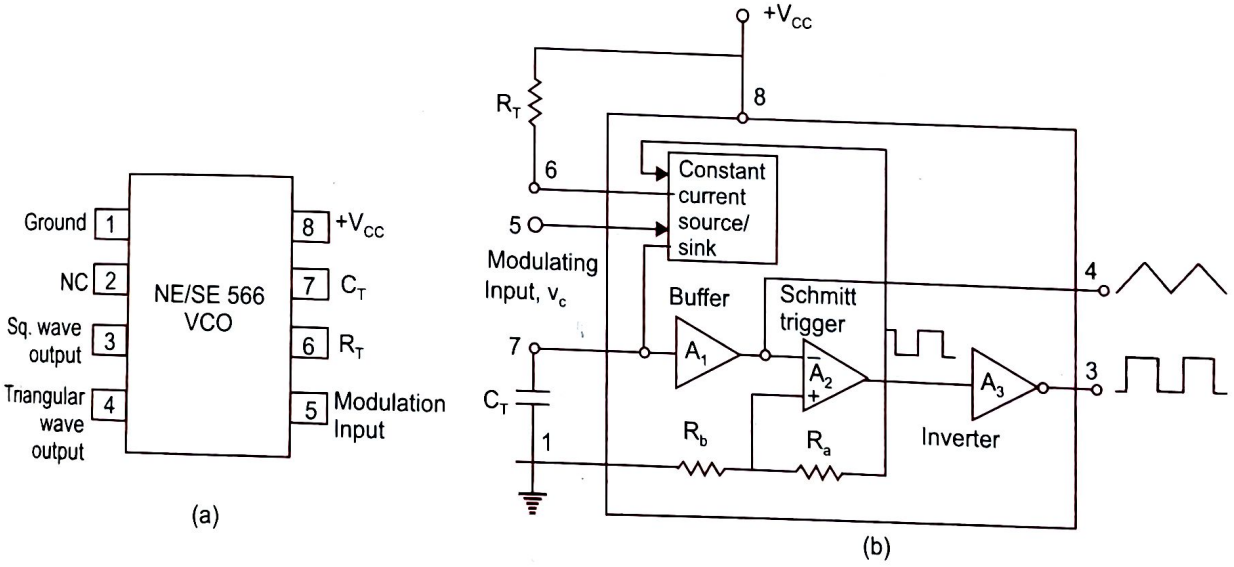

Fig. 10.7 Voltage controlled oscillator (a) Pin configuration, (b) Block diagram

A small capacitor of .001 μF should be connected between pin 5 and 6 to eliminate possible oscillations. A VCO is commonly used in converting low frequency signals such as EEGs, EKG into an audio frequency range. These audio signals can be transmitted over telephone lines or a two way radio communication systems for diagnostic purposes or can be recorded on a magnetic tape for further reference.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{CC} and 0.5 V_{CC}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{CC} to 0.25 V_{CC}. In Fig. 10.7 (c), when the voltage on the capacitor C_T exceeds 0.5 V_{CC} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{CC}). The capacitor now discharges and when it is at 0.25 V_{CC}, the output of Schmitt trigger goes HIGH (V_{CC}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The inverter A_3 is basically a current amplifier used to drive the load. The output waveforms are shown in Fig. 10.7 (c).

The output frequency of the VCO can be calculated as follows:

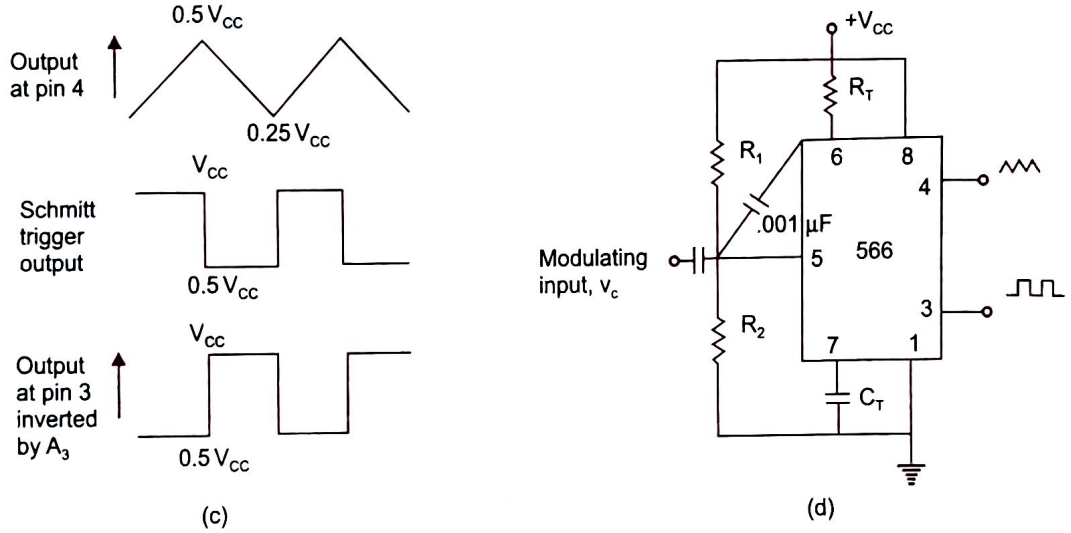

Fig. 10.7 (c) Output waveform, (d) Typical connection diagram

The total voltage on the capacitor changes from 0.25 V_{CC} to 0.5 V_{CC}. Thus $\Delta v = 0.25\ V_{CC}$. The capacitor chargers with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25\ V_{CC}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\ V_{CC} C_T}{i} \tag{10.8}$$

The time period T of the triangular waveform = $2\Delta t$. The frequency of oscillator f_0 is,

$$f_0 = \frac{1}{T} = \frac{1}{2\,\Delta t} = \frac{i}{0.5\ V_{CC} C_T}$$

But,
$$i = \frac{V_{CC} - v_c}{R_T} \tag{10.9}$$

where, v_c is the voltage at pin 5. Therefore,

$$f_0 = \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} \tag{10.10}$$

The output frequency of the VCO can be changed either by (i) R_T, (ii) C_T or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit as shown in Fig. 10.7 (d). The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{CC} to V_{CC} which can produce a frequency variation of about 10 to 1. With no modulating input signal, if the voltage at pin 5 is biased† at (7/8) V_{CC}, Eq. (10.10) gives the VCO output frequency as,

† The expression of f_0 depends upon the initial choice of the voltage v_c. If the value of v_c is taken as 0.85 V_{CC} then f_0 comes out to be $0.3/R_TC_T$.

$$f_o = \frac{2(V_{CC} - (7/8)V_{CC})}{C_T R_T V_{CC}} = \frac{1}{4R_T C_T} = \frac{0.25}{R_T C_T} \tag{10.11}$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_o}{\Delta v_c}$$

Here Δv_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o = \frac{2(V_{CC} - v_c + \Delta v_c)}{C_T R_T V_{CC}} - \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} = \frac{2\Delta v_c}{C_T R_T V_{CC}} \tag{10.12}$$

or, $$\Delta v_c = \frac{\Delta f_o C_T R_T V_{CC}}{2} \tag{10.13}$$

Putting the value of $C_T R_T$ from Eq. (10.11)

$$\Delta v_c = \Delta f_o V_{CC}/8f_o \tag{10.14}$$

or, $$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8 f_o}{V_{CC}} \tag{10.15}$$

Example 10.1

In a VCO, if input signal frequency f_s = 20 kHz, free running, frequency f_o = 21 kHz/V, voltage to frequency conversion factor K_V is 4 kHz/V, find the change in the dc control voltage V_c during lock.

Solution

The voltage to frequency conversion factor

$$K_v = \frac{\Delta f_o}{\Delta V_C}$$

So, $$\Delta V_C = \frac{\Delta f_o}{K_v}$$

Frequency shift $$\Delta f_o = 21 \text{ kHz} - 20 \text{ kHz}$$
$$= 1 \text{ kHz}$$

Therefore $$\Delta V = \frac{1 \times 10^3}{4 \times 10^3} V$$

$$= 0.25 \text{ V}.$$

10.5 LOW PASS FILTER

The filter used in a PLL may be either passive type as shown in Fig. 10.8 (a, b) or active type as in Fig. 10.8 (c).

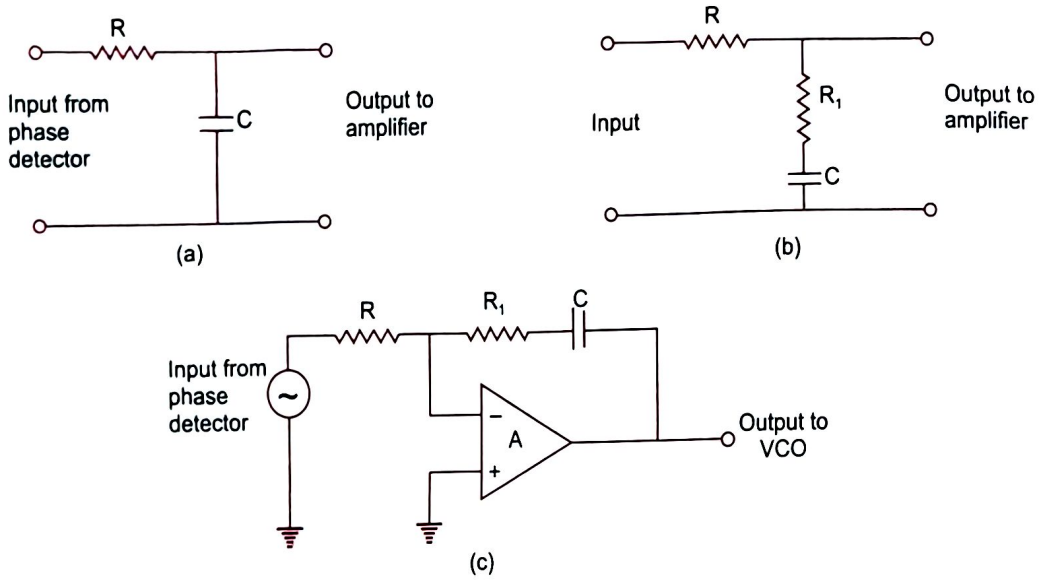

Fig. 10.8 (a) Low pass filter, (b) Passive filter, (c) Active filter

The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. These characteristics include capture and lock range, band-width and transient response. If filter band-width is reduced, the response time increases. However, reducing the band-width of the filter also reduces the capture range of the PLL. The filter serves one more important purpose. The charge on the filter capacitor gives a short time 'memory' to the PLL. Thus, even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.

Example 10.2

The free running frequency of a PLL is 300 kHz and the bandwidth of the low pass filter is 10 kHz. Will the PLL acquire lock for an input signal of 320 kHz. Also what happens if the cut-off frequency of the LPF is 25 kHz.

Solution

The phase detector outputs will be

$$f_s + f_0 = 320 \text{ kHz} + 300 \text{ kHz}$$
$$= 620 \text{ kHz}$$

and $$f_s - f_o = 320 \text{ kHz} - 300 \text{ kHz}$$
$$= 20 \text{ kHz}$$

If the bandwidth of the LPF is 10 kHz, then PLL will not lock. However, for 25 kHz BW. PLL will lock.

10.6 MONOLITHIC PHASE-LOCKED LOOP

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However, a number of manufacturers have introduced monolithic PLLs too. Some of the important monolithic PLLs are SE/NE560 series introduced by Signetics and LM560 series by National Semiconductor. The SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. Since 565 is the most commonly used PLL, we will discuss some of the important features of this IC chip.

IC PLL 565

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in Fig. 10.9 (a, b). The output frequency of the VCO (both inputs 2, 3 grounded) as given by Eq. (10.11) can be rewritten as,

$$f_o = \frac{0.25}{R_T C_T} \text{ Hz} \qquad (10.16)$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and the phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 kΩ.

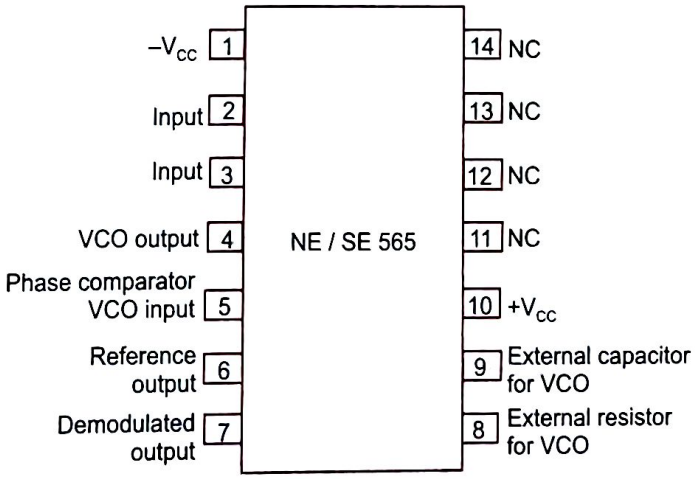

Fig. 10.9 (a) Pin diagram

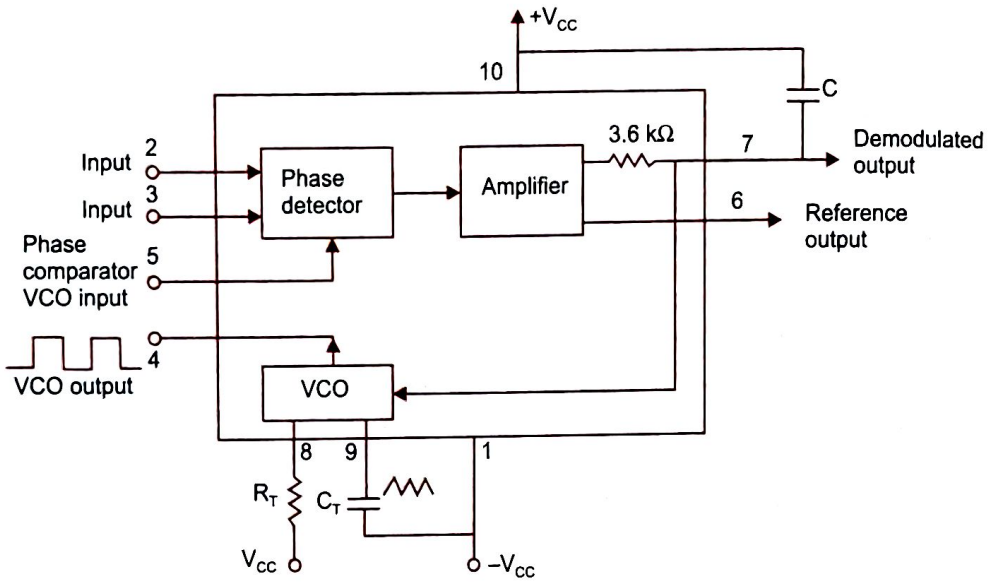

Fig. 10.9 (b) NE/SE565 PLL block diagram

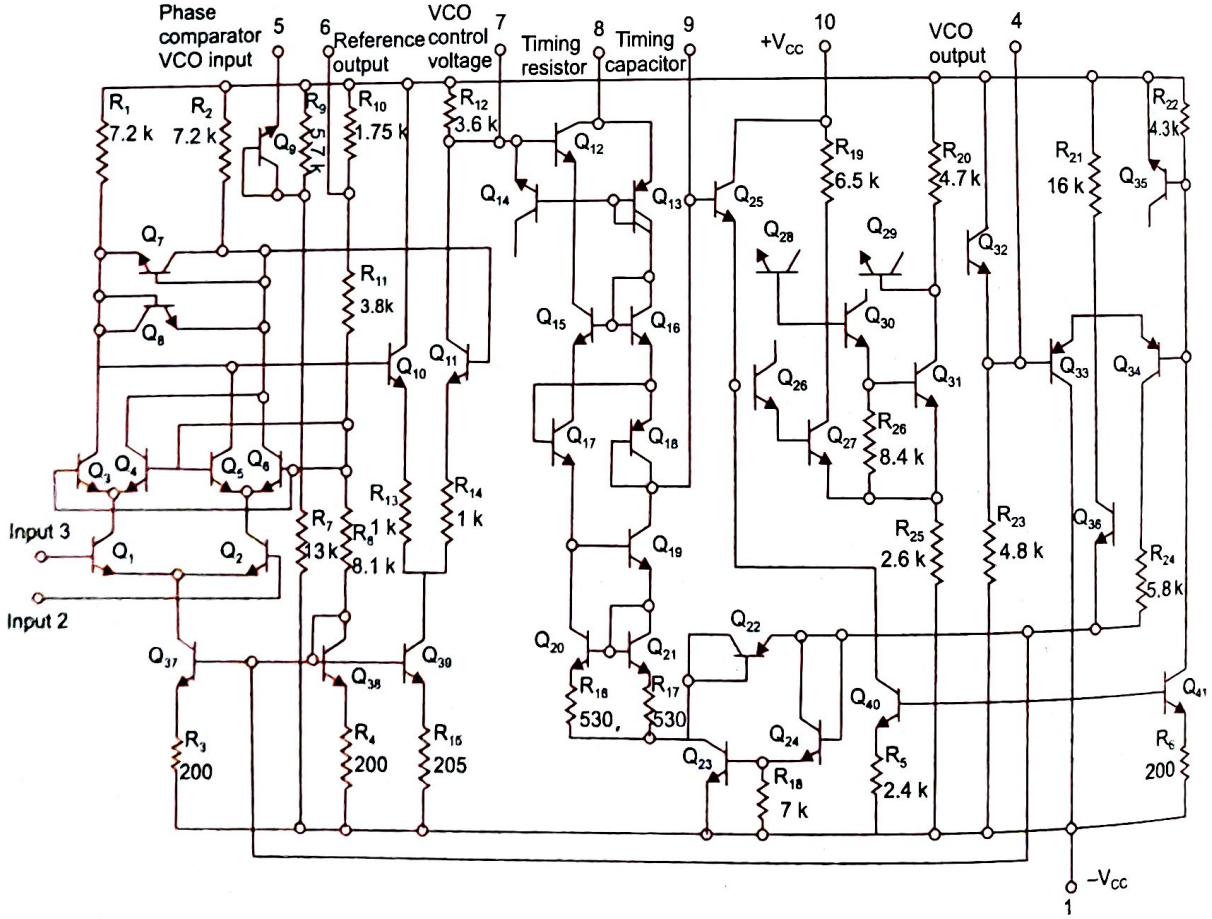

Fig. 10.10 Circuit diagram of LM565 PLL

In Fig. 10.10, a complete diagram of LM565 (National Semiconductor) IC PLL is presented. The analog phase detector is comprised of the Q_1–Q_2, Q_3–Q_4 and Q_5–Q_6 differential amplifier pairs with Q_{37} together with R_3 (200 Ω) serving as a current sink bias source. Resistors R_1 and R_2 (each 7.2 kΩ) serve as the load for the phase detector. The output voltage of the phase detector is limited by the diode-connected transistors Q_7 and Q_8 to a maximum of ±0.7 V which minimizes the effect of high amplitude noise pulses and other transient effect on the operation of the PLL. This makes the conversion ratio of the phase detector of 565 PLL as,

$$K_\phi = \frac{0.7-(-0.7)}{\pi} = \frac{1.4}{\pi} \tag{10.17}$$

A balanced output is taken from the phase detector and supplied to the Q_{10}–Q_{11} differential pair which is biased by the Q_{39} current sink. Q_{10}–Q_{11} serves as the amplifier stage (which is designed for a gain of 1.4) after phase detector. A single ended output is taken from this stage across the resistors R_{12} (3.6 kΩ). Resistor R_{12} also serves as part of the LPF when an external capacitor between pin 7 and ground of is connected.

The VCO consists of a voltage controlled current source (Q_{12} through Q_{23}). Equal charging and discharging currents are supplied to external capacitor C_T connected at pin 9. Resistor R_T is connected between pin 8 and positive supply $+V_{CC}$. The Schmitt trigger (Q_{25} through Q_{36}) with the differential amplifier output circuit (Q_{33} and Q_{34}) is part of VCO. This controls the turn-on and turn-off of Q_{23} and Q_{24} for the switching action of the current source for the charging and discharging cycles. Transistor Q_{14}, Q_{26}, Q_{30}, Q_{35} are used as diodes to obtain the desired level shift.

The important electrical parameters of 565 PLL are:

Operating frequency range	:	0.001 Hz to 500 kHz
Operating voltage range	:	±6 V to ±12 V
Input level	:	10 mV rms min. to 3 V pp max
Input impedance	:	10 kΩ typical
Output sink current	:	1 mA typical
Drift in VCO centre frequency with temperature	:	300 ppm/°C. (parts per million per degree centigrade)
Drift in VCO centre frequency with supply voltage	:	1.5 per cent/V max
Triangle wave amplitude	:	2.4 V_{pp} at ±6 V supply voltage
Square wave amplitude	:	5.4 V_{pp} at ±6 V supply voltage
Bandwidth adjustment range	:	< ±1 to ±60%

Derivation of Lock-in Range

If ϕ radians is the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by,

$$v_c = K_\phi(\phi - \pi/2) \tag{10.18}$$

where K_ϕ is the phase angle-to-voltage transfer coefficient of the phase detector. The control voltage to VCO is,

$$v_c = AK_\phi(\phi - \pi/2) \tag{10.19}$$

where A is the voltage gain of the amplifier. This v_c shifts VCO frequency from its free running frequency f_0 to a frequency f given by,

$$f = f_o + K_v v_c \tag{10.20}$$

where K_v is the voltage to frequency transfer coefficient of the VCO. When PLL is locked-in to signal frequency f_s, then we have

$$f = f_s = f_o + K_v v_c \tag{10.21}$$

since, $$v_c = (f_s - f_o)/K_v = A K_\phi (\phi - \pi/2) \tag{10.22}$$

Thus, $$\phi = \pi/2 + (f_s - f_o)/K_v K_\phi A \tag{10.23}$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian (see in Fig. 10.4 (c) and $v_{e(max)} = \pm K_\phi \pi/2$ from Eq. 10.6. The corresponding value of the maximum control voltage available to drive the VCO will be,

$$v_{c(max)} = \pm (\pi/2) K_\phi A \tag{10.24}$$

The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_o)_{max} = K_v v_{c(max)} = K_v K_\phi A (\pi/2) \tag{10.25}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_o \pm (f - f_o)_{max} = f_o \pm K_v K_\phi (\pi/2) A = f_o \pm \Delta f_L \tag{10.26}$$

where $2 \Delta f_L$ will be the lock-in frequency range and is given by,

lock-in range = $$2 \Delta f_L = K_v K_\phi A \pi \tag{10.27}$$

or, $$\Delta f_L = \pm K_v K_\phi A (\pi/2) \tag{10.28}$$

The lock-in range is symmetrically located with respect to VCO free running frequency f_o. For IC PLL 565,

$$K_v = \frac{8 f_o}{V} \quad \text{(from Eq. 10.15)}$$

where $$V = +V_{CC} - (-V_{CC})$$

Again, $$K_\phi = \frac{1.4}{\pi} \quad \text{(from Eq. 10.17)}$$

and $$A = 1.4$$

Hence the lock-in range from Eq. 10.28 becomes,

$$\Delta f_L = \pm 7.8 f_o/V \tag{10.29}$$

Derivation of Capture Range

Initially, when PLL is not locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be,

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o) t + \Delta\theta \tag{10.30}$$

thus the phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \tag{10.31}$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi(\pi/2)$ and a fundamental frequency $(f_s - f_o) = \Delta f$.

The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)} \tag{10.32}$$

where $f_1 = 1/2\,\pi\,RC$ is the 3-dB point of LPF. In the slope portion of LPF where $(f/f_1)^2 >> 1$, then

$$T(f) \simeq \frac{f_1}{jf} \tag{10.33}$$

The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_o$. If $\Delta f > 3f_1$, the LPF transfer function will be approximately,

$$T(\Delta f) \simeq f_1/\Delta f = f_1/(f_s - f_o) \tag{10.34}$$

The voltage v_c to drive the VCO is,

$$v_c = v_e \times T(f) \times A \tag{10.35}$$

or,
$$v_{c(max)} = v_{e(max)} \times T(f) \times A$$
$$= \pm K_\phi (\pi/2) A\,(f_1/\Delta f). \text{ (from Eq. (10.24))} \tag{10.36}$$

Then the corresponding value of the maximum VCO frequency shift is,

$$(f - f_o)_{max} = K_v\, v_{c(max)} = \pm K_v K_\phi (\pi/2) A\,(f_1/\Delta f) \tag{10.37}$$

For the acquisition of signal frequency, we should put $f = f_s$, so that the maximum signal frequency range that can be acquired by PLL is,

$$(f_s - f_o)_{max} = \pm K_v K_\phi (\pi/2) A\,(f_1/\Delta f_c) \tag{10.38}$$

Now
$$\Delta f_c = (f_s - f_o)_{max}$$

so,
$$(\Delta f_c)^2 = K_v K_\phi (\pi/2) A f_1 \text{ (from Eq. (10.38))}$$

since,
$$\Delta f_L = \pm K_v K_\phi (\pi/2) A$$

we get,
$$(\Delta f_c) \simeq \pm\sqrt{f_1\, \Delta f_L} \tag{10.39}$$

Therefore, the total capture range is,

$$2\,\Delta f_c \simeq 2\sqrt{f_1\, \Delta f_L} \tag{10.40}$$

where the lock-in range $= 2\,\Delta f_L = K_v\, K_\phi\, A\,\pi$. In case of IC PLL 565, $R = 3.6$ kΩ, so the capture range is

$$\pm\left[\frac{\Delta f_L}{2\pi(3.6 \times 10^3)\,C}\right]^{\frac{1}{2}} \tag{10.41}$$

where C is in farads.

The capture range is symmetrically located with respect to VCO free running frequency f_o as is shown in Fig. 10.11. The PLL cannot acquire a signal outside the capture range, but

once captured, it will hold on till the signal frequency goes beyond the lock-in range. In order to increase the ability of lock-in range, large capture range is required. However, a large capture range will make the PLL more susceptible to noise and undesirable signal. Hence a suitable compromise is often reached between these two opposing requirements of the

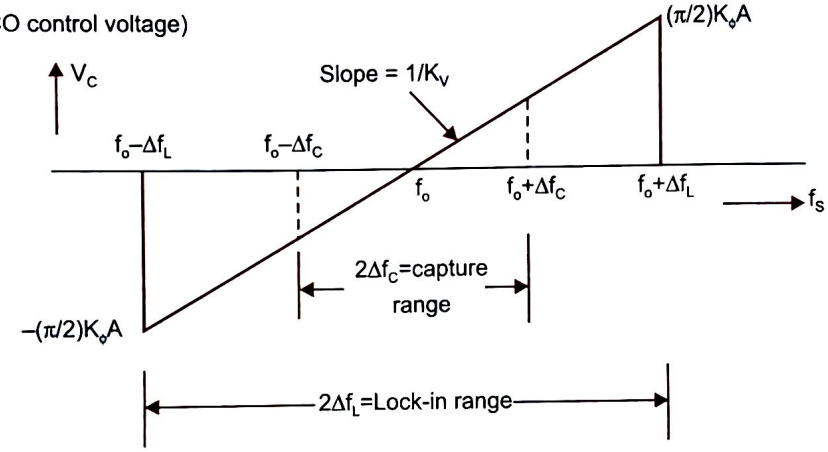

Fig. 10.11 PLL lock-in range and capture range

capture range. Many a times the LPF band-width is first set for a large value for initial acquisition of signal, then once the signal is captured, the band-width of LPF is reduced substantially. This will minimize the interference of undesirable signals and noise.

Example 10.3

The free running frequency of a 565 PLL is 100 kHz, the filter capacitar is 2μF and supply voltage is ± 6V. Compute the lock-in-range, capture range frequency and the value of external components R_T & C_T.

Solution

Given f_o = 100 kHz, C = 2μF and V_{CC} = ± 6V.

We know that the lock-in range is given by

$$\Delta f_L = \pm \frac{7.8 f_o}{V} \qquad \text{[from Eq. (10.29)]}$$

$$= \pm \frac{7.8 f_o}{V_{CC} - (-V_{CC})}$$

$$= \pm \frac{7.8 \times 100}{6 - (-6)V} = \pm 65 \text{ kHz}$$

Thus lock-in range = ± 65 kHz

The capture range, $2\Delta f_C$ is given by

$$2\Delta f_C = \pm \sqrt{\frac{\Delta f_L}{2\pi(\times 3.6 \times 10^3)C}} \qquad \text{[from Eq. (10.41)]}$$

Putting the values and solving, we get

$$2\Delta f_C = 2.397 \text{ kHz}$$

Further, the free running frequency, f_o is

$$f_o = \frac{0.25}{R_T C_T} \qquad \text{[from Eq. (10.16)]}$$

Assuming $R_T = 10\text{K}\Omega$, we obtain

$C_T = 250$ pF.

Example 10.4

Compute the free running frequency f_o, lock-in range and capture range of PLL 565. Assume $R_T = 20$ KΩ, $C_T = 0.01$ μF, $C = 1$ μF and supply voltage is ± 6V.

Solution

Given $R_T = 10$ KΩ, $C_T = 0.01$ μF and $C = 1\mu$F

The free running frequency of VCO is

$$f_o = \frac{0.25}{R_T C_T} = \frac{0.25}{10 \times 10^3 \times 0.01 \times 10^{-6}}$$

$$= 2.5 \text{ kHz}$$

The lock in range is given by

$$\Delta f_L = \pm \frac{7.8 f_o}{V} = \pm \frac{7.8 \times 2.5 \times 10^3}{12}$$

$$= 1.62 \text{ kHz}$$

The capture range is given by

$$2\Delta f_C = \sqrt{\frac{\Delta f_L}{2\pi \times (3.6 \times 10^3) C}}$$

$$= \sqrt{\frac{2 \times 1.62 \times 10^3}{2\pi \times (3.6 \times 10^3) \times 1 \times 10^{-6}}}$$

$$= 378 \text{ Hz}$$

10.7 PLL APPLICATIONS

The output from a PLL system can be obtained either as the voltage signal $v_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator application whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

Consider the case of voltage output. When PLL is locked to an input frequency, the error voltage $v_c(t)$ is proportional to $(f_s - f_o)$. If the input frequency is varied as in the case of FM signal, v_c will also vary in order to maintain the lock. Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one particular frequency component at the input. The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals.

Some of the typical applications of PLL are discussed now.

10.7.1 Frequency Multiplication/Division

Figure 10.12 gives the block diagram of a ***frequency multiplier*** using PLL. A divide by N network is inserted between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_0 is given by,

$$f_0 = N f_s \tag{10.42}$$

The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

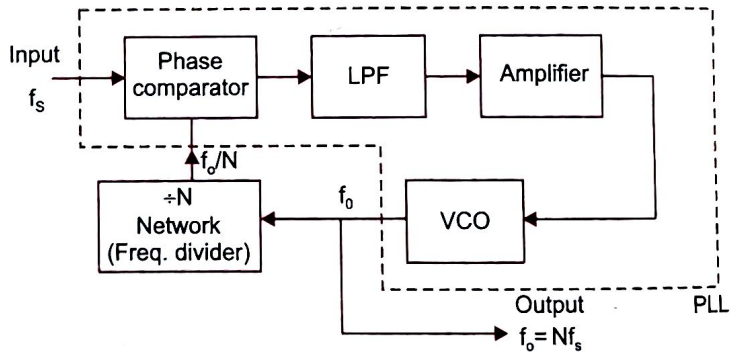

Fig. 10.12 Frequency multiplier using IC PLL

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.

The circuit of Fig. 10.12 can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output f_0 of VCO is now given by

$$f_0 = \frac{f_s}{m} \tag{10.43}$$

10.7.2 Frequency Translation

A schematic for shifting the frequency of an oscillator by a small factor is shown in Fig. 10.13. It can be seen that a mixer (or multiplier) and a low pass filter are connected externally to the PLL. The signal f_s which has to be shifted and the output frequency f_0 of the VCO are applied as inputs to the mixer. The output of the mixer contains the sum and difference of f_s and f_0. However, the output of LPF contains only the difference signal $(f_0 - f_s)$. The translation or offset frequency $f_1 (f_1 << f_s)$ is applied to the phase comparator. When PLL is in locked state,

$$f_0 - f_s = f_1$$

or

$$f_0 = f_s + f_1 \tag{10.44}$$

Thus, it is possible to shift the incoming frequency f_s by f_1.

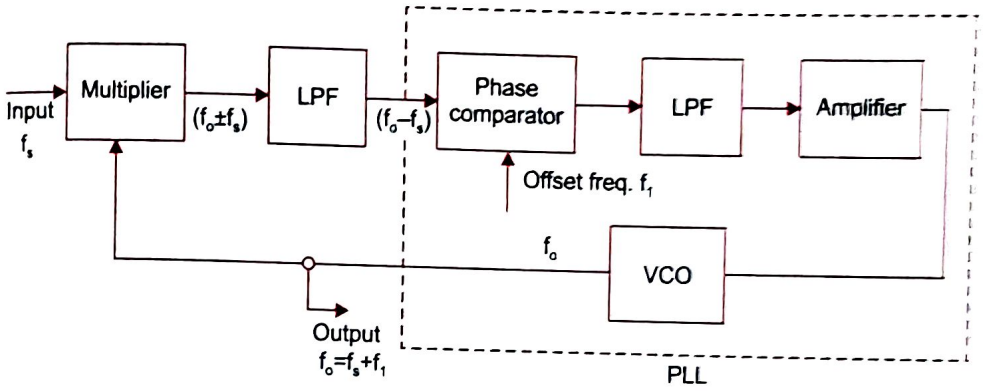

Fig. 10.13 PLL used as a frequency translator

10.7.3 AM Detection

A PLL may be used to demodulate AM signals as shown in Fig. 10.14. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

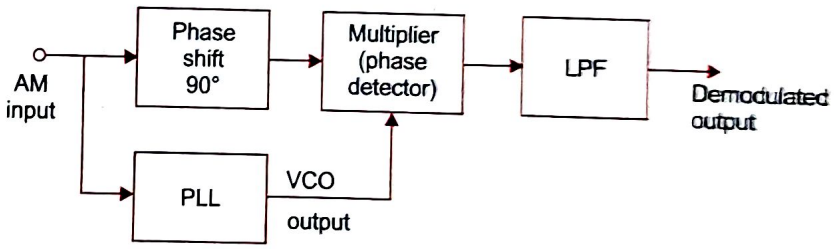

Fig. 10.14 PLL used as AM demodulator

10.7.4 FM Demodulation

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

10.7.5 Frequency Shift Keying (FSK) Demodulator

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved

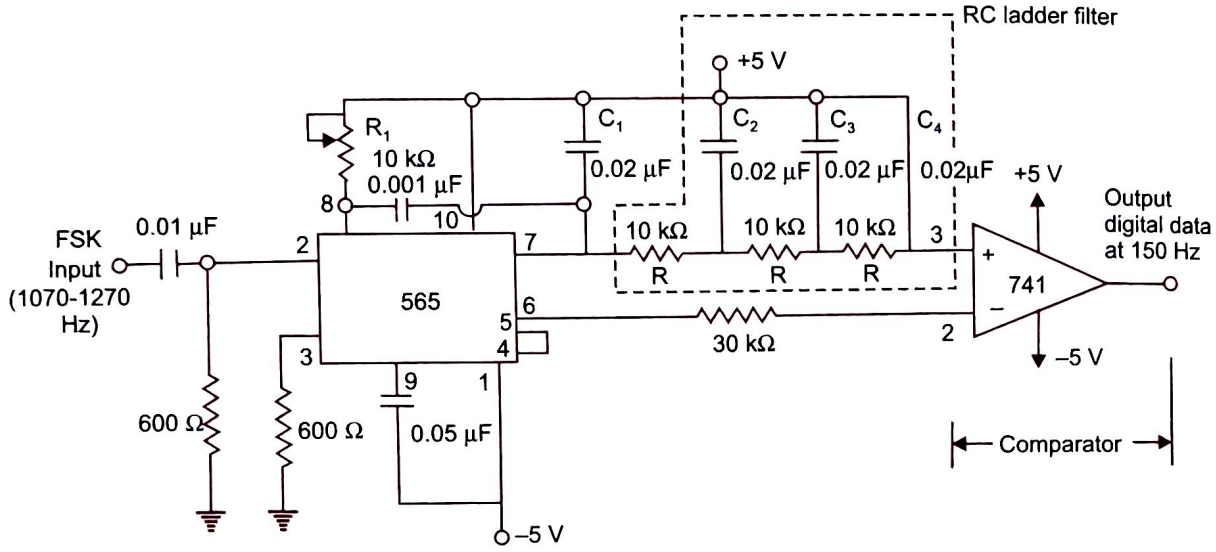

Fig. 10.15 FSK demodulator

using a FSK demodulator at the receiving end. The 565 PLL is very useful as a FSK demodulator. Figure 10.15 shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

SUMMARY

1. A phase locked loop consists of a phase detector, low pass filter, amplifier and a VCO in feedback loop.
2. The important characteristics of a PLL are: lock-in range, capture range and pull-in-time.
3. The lock-in range is usually greater than the capture range. The capture range depends upon the LPF characteristics.
4. The phase detectors are of two types: analog and digital. The phase detector is basically a multiplier.
5. The frequency of VCO can be set by an external capacitor and resistor. The output frequency f_0 of VCO is compared with the incoming signal f_s. When $f_0 = f_s$, the PLL is said to be locked.
6. The low pass filter may be passive or active type. The LPF controls the capture range and lock range of PLL.
7. Signetics SE/NE 560 series – 560, 561, 562, 564, 565 and 567 are monolithic PLLs. All the blocks of a PLL are also available as independent ICs and can be interconnected to make a PLL.
8. The PLLs are used as frequency multiplier, divider, AM and FM demodulator, FSK demodulator etc.

REVIEW QUESTIONS

10.1. List the basic building blocks of a PLL.
10.2. Define capture range, lock-in range and pull-in-time.
10.3. Which is greater 'Capture range' or 'Lock-in range'?

10.4. What is the major difference between digital and analog PLLs?
10.5. Give the block diagram of IC 566 VCO and explain its operation.
10.6. What is the range of modulating input voltage applied to a VCO?
10.7. List the applications of PLL.
10.8. Draw the circuit of a PLL AM detector and explain its operation.

PROBLEMS

10.1. In the VCO of Fig. 10.7 calculate the change in output frequency if the supply voltage is varied between 9 V and 11 V. Assume V_{cc} = 12 V, R_T = 6.8 kΩ, C_T = 75 pF, R_1 = 15 kΩ and R_2 = 100 kΩ.
10.2. Determine the dc control voltage v_c at lock if signal frequency f_s = 10 kHz, VCO free running frequency is 10.66 kHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/V.
10.3. If f_s = 100 kHz, the voltage to frequency transfer coefficient of VCO, K_v = 2 MHz/V, f_0 the VCO frequency is 5 MHz and N = 100 in the frequency multiplier of Fig. 10.12, what is the dc control voltage at lock?
10.4. Calculate output frequency f_0, lock range Δf_L and capture range Δf_c of a 565 PLL if R_T = 10 kΩ, C_T = 0.01 μF and C = 10 μF.
10.5. Repeat Problem 10.4 for C_T = 470 pF.

EXPERIMENT

(a) To study the operation of NE 565 PLL.
(b) To use NE 565 as a multiplier.

PROCEDURE

1. Make connections of the PLL as shown in Fig. E. 10.1 (a).
2. Measure the free running frequency of VCO at pin 4, with the input signal V_{in} set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$.
3. Now apply the input signal of 1 V_{pp} square wave at a 1 kHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.

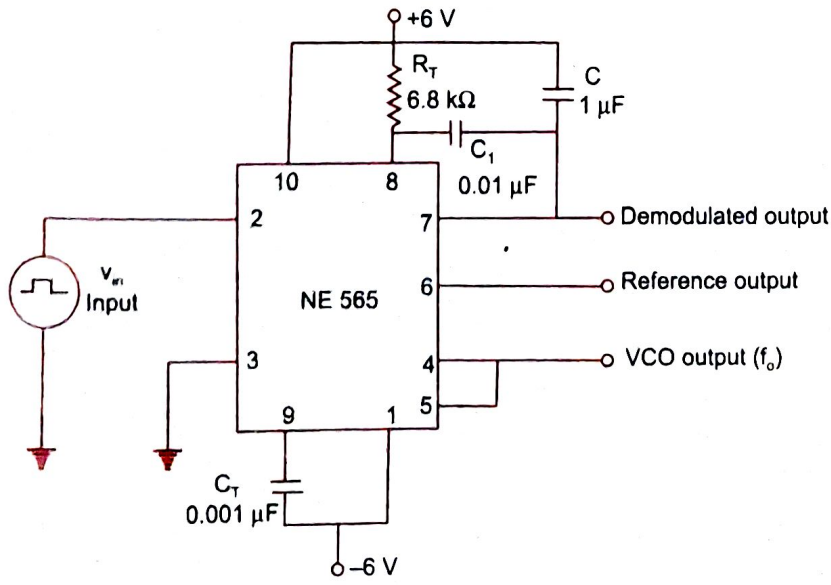

Fig. E. 10.1 (a) NE565 PLL connection diagram

4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency f_2. This frequency f_2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f_3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range.
6. The lock-in range $\Delta f_L = (f_2 - f_4)$. Compare it with the calculated value of $\frac{\pm 7.8 f_o}{12}$. Also the capture range is $\Delta f_c = (f_3 - f_1)$. Compare it with the calculated value of capture range.

$$\Delta f_c = \pm \left[\frac{\Delta f_L}{(2\pi)(3.6)(10^3) \times C} \right]^{\frac{1}{2}}$$

7. To use PLL as a multiplier, make connections as shown in Fig. E. 10.1 (b). The circuit uses a 4-bit binary counter 7490 used as a divide-by-5 circuit.

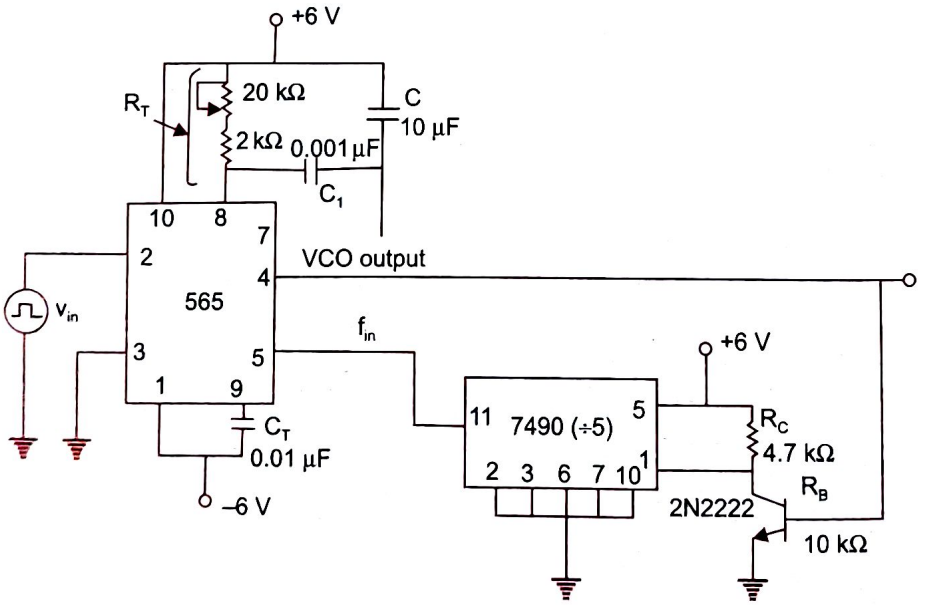

Fig. E. 10.1 (b) NE 565 as a frequency multiplier

8. Set the input signal at 1 V_{pp} square wave at 500 Hz.
9. Vary the VCO frequency by adjusting the 20 kΩ potentiometer till the PLL is locked. Measure the output frequency. It should be 5 times the input frequency.
10. Repeat steps 8, 9 for input frequency of 1 kHz and 1.5 kHz.